RISC-V at Bluespec

Presentation @ RISC-V workshop, Jan 14-15, 2015, Monterey CA

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Briefly ...

- Bluespec, Inc. is opening a new business front involving tightly-coupled hardware-software apps (embedded, IoT, some HPC)
  - Hardware accelerators for speed and energy-efficiency, especially for new, high-complexity algorithms (e.g., HD video, new crypto)
  - CPU/SoC essential (but raw CPU performance not crucial, at least initially)

- Our “in-house” processor components will be RISC-V
  - (Although, by using standard AXI for interconnect, customers can substitute other CPUs if they prefer.)

- We expect many of our components to be open-source
  - Our business model is focused more on pre-tested, pre-certified, pre-integrated, curated systems (similar to Red Hat model)
  - Off-the-shelf offerings, but also custom on request

Today at the RISC-V workshop:
- This talk: quick overview of RISC-V development at Bluespec
  - Cissr simulator, BluROCS synthesizable simulator, Flute pipelined implementation
  - SoC structure around the CPU
  - GDB support, Tandem Verification

- Posters/demo later today: Showing some of these in action
Overview of Bluespec’s RISC-V components

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<table>
<thead>
<tr>
<th>Cissr</th>
<th>BluROCS</th>
<th>Flute</th>
</tr>
</thead>
<tbody>
<tr>
<td>C ISS (instruction set simulator)</td>
<td>BSV ISS (instruction set simulator)</td>
<td>BSV Pipeline</td>
</tr>
</tbody>
</table>

(Details follow)
## Current Bluespec RISC-V CPU implementations

<table>
<thead>
<tr>
<th>Implementation</th>
<th>Cissr</th>
<th>BluROCS</th>
<th>Flute</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source language</td>
<td>C (some C++)</td>
<td>BSV</td>
<td>BSV</td>
</tr>
<tr>
<td>Type of implementation</td>
<td>ISS (instruction set simulator)</td>
<td>ISS</td>
<td>6-stage pipeline, single-issue, in-order, branch-prediction</td>
</tr>
<tr>
<td>Synthesizable? (FPGA-able?)</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>SoC connectivity</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Linux boot time in simulation</td>
<td>Few seconds</td>
<td>Many hours</td>
<td>Many hours</td>
</tr>
<tr>
<td>Linux boot-time on FPGA</td>
<td>N/A</td>
<td>Seconds</td>
<td>Fewer seconds</td>
</tr>
</tbody>
</table>

All three components:
- Run ELF binaries
- Boot Linux kernel
  - Handle Exceptions
  - Have MMUs
  - Have su/user modes
- Have direct GDB support
- Support RV32 and RV64

Both run on FPGAs

Trivia:
- “Cissr” = “C Instruction Set Simulator for RISC-V”
- “BluROCS” = “Bluespec RISC-V Order Code Simulator”
- “Flute” = “A pipe that makes beautiful music”

¹ Early British Computers (1940s-1950s) used the term “Order Code” for what we call an Instruction Set.
Direct GDB support

- GDB can (standardly) be run remotely, i.e., can debug a remote process
  - Uses a remote `gdb stub` that serves standard GDB RSP (Remote Serial Protocol) (r/w registers, r/w mem, set/rm breakpoints, continue, step, …)
  - This is all pure software
  - Perfectly adequate if your CPU/HW system/OS kernel are all stable
  - But what if you’re developing a CPU/system/OS kernel that are not yet stable?

- We’ve developed a `gdb stub` in hardware hooking directly into the CPU (BluROCs/Flute)
  - “Rock to stand on, while you investigate shifting sands”

Terminal window running riscv-gdb

On host computer

Bluesim simulator, or FPGA

TCP/IP if simulation

PCle/BlueNoC if FPGA

SoC

TCP/IP carrying standard “gdb remote serial protocol” (RSP)
Tandem verification catches divergence immediately and is built into BluROCS and Flute.
Written for high reuse / adaptation / evolution
- Written entirely in BSV: excellent track record of reuse / adaptation / evolution due to
  - Very strong typing and parameterizability (Haskell-like)
  - Scalable concurrency (globally atomic transactions) with object-oriented modularity
- BluROCS and Flute have exactly the same HW interface (completely plug-compatible)
- Flute is written in latency-insensitive style
  - Conceptually, the pipeline stages form a “distributed system”
  - Inter-stage communication is logically “message-passing”; latency does not affect correctness
  - Easy to replace/change/stretch stages
  - Enables: evolution, physical silicon layout, and modular formal verification
Exploring Formal Verification

• For:
  • Flute (and future pipelined implementations of RISC-V)
  • Un-core components: MMUs, Caches, interconnects, coherence
  • Accelerators and accelerated computations

• Leveraging:
  • BSV rule semantics
  • Latency-insensitive style (which we believe can enable modular and therefore scalable proofs)
  • Existing past work in using FV of CPU pipelines and cache coherence protocols using BSV predecessors (with same rule semantics)

• Have had initial conversations with at least two interested parties in academia/research-labs
  • Please let us know if you have an interest in studying something like this
RISC-V software activities

- Already made several contributions to the open-source repos:
  - riscv-gcc: mods for “soft-float” (emulated floating point) and no-atomic-memory-ops
  - riscv-gdb: port of gdb for RISC-V
  - Components of RV32 support in riscv-gnu-toolchain and riscv-linux repos

- Adapted Linux kernel to run on Cissr/BluROCS/Flute

- Next:
  - Will also be looking beyond Linux kernel to a full-blown Linux distro (Debian? Android?)
    - Also to be contributed into the open-source repo
    - Coordinate with anyone else doing this
RISC-V evangelism

• Bluespec advocated and helped persuade the upcoming “India Microprocessor Project” to base itself on RISC-V (we’ve been talking to them about this since March 2013).

• Bluespec suggested to IIT Chennai, India, to adopt RISC-V (see Neel Gala’s talk in this workshop)

• Bluespec has other partners, both commercial and R&D, with whom also we are making this case
Next: Infrastructure for tightly coupled HW accelerators

Goal: rapid development of tightly-coupled HW accelerators for new, complex algorithms, for speed and energy efficiency

Host side

- App superstructure in C/C++/your favorite PL
- BlueNoC/Connectal
- PCIe/AXI/…

HW side

- Computation kernels in BSV/your favorite HDL
- BlueNoC/Connectal
- PCIe/AXI/…

Automatically generated infrastructure, based on user-code SW/HW interfaces and chosen Host/HW platform (ready-to-run on a wide variety of FPGA boards)

Bluespec infrastructure:
- Transactors (TLM, Get/Put, …)
- Clock control, HW breakpoints and visibility
- BlueNoC host-FPGA multipoint network
- PCIe support for many FPGA boards

Connectal: open-source BSV from Quanta
- Efficient RPC and direct memory access
- https://github.com/cambridgehackers/connectal
- FPGA’15, February 22–24, 2015, Monterey, CA

Software-Driven Hardware Development

Myron King, Jamey Hicks, John Ankcorn
Quanta Research Cambridge
{myron.king,jamey.hicks,john.ankcorn}@qclab.com
End
System setup for today’s demo is similar to this.

- Host running Linux
- PCIe link
- FPGA boards: KC705/VC707/DINI/HyperSilicon/TBD
  - Pictured: DINI Xilinx Kintex-7 410T ~3M ASIC gates

Today’s Demo: Lenovo Thinkpad, Xilinx VC707 board
We’re connecting remotely using VNC.
Demo: BluROCS/Flute running on FPGA

Start multiple terminal windows

Linux Laptop

riscv-gdb

% riscv-gdb
...

TCP/IP

% gdbstub
...

XIilinx VC707 FPGA board

Here:
- Load an ELF binary
- Set a breakpoint
- Run until breakpoint
- Examine source

% htif-proxy
Hello, World!

console I/O

Here:
- Download bitfile
- Start FPGA comms

TCP/IP

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BluROCS/Flute

FPGA

I/MMU
DCache
Interconnect Fabric
Memory interface
FPGA Board
DRAM

PCIe

Bluespec Transactors

Cissr
ISS behavior
Architectural State

Bluespec SceMi libraries
Bluespec BlueNoC driver
Linux PCIe

Transactors

Bluespec SceMi
Bluespec BlueNoC
Bluespec PCIe