

# **Pydgin for RISC-V: A Fast and Productive Instruction-Set Simulator**

Berkin Ibeyi

In collaboration with Derek Lockhart (Google), and Christopher Batten

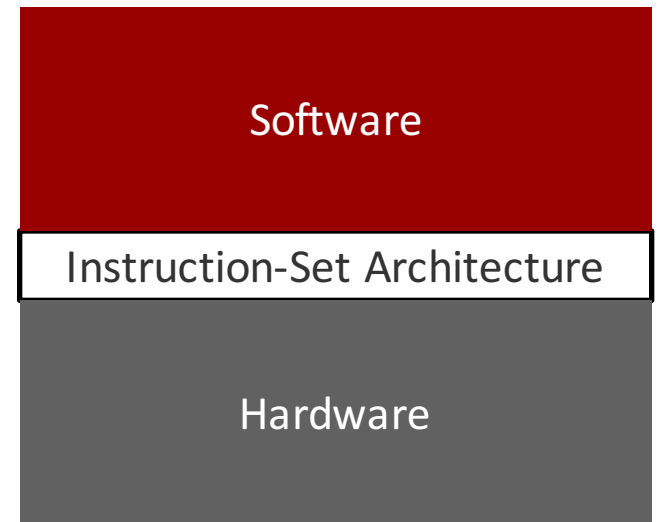
3rd RISC-V Workshop, Jan 2016



Cornell University  
Computer Systems Laboratory

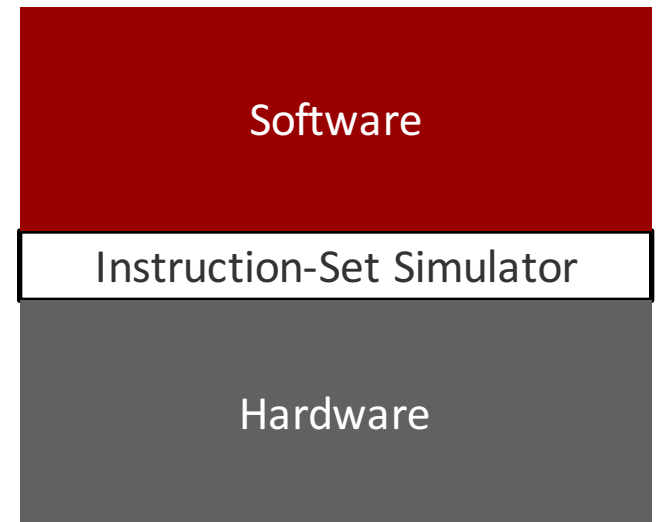
# Motivation

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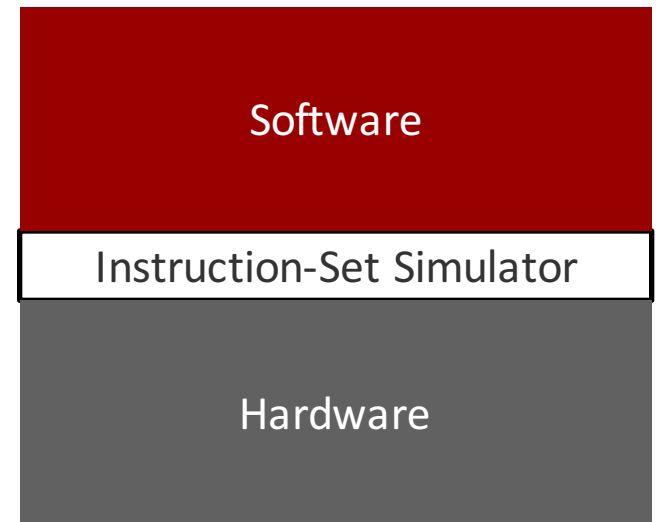


# Motivation

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## Performance

Interpretive: 1-10 MIPS (1-10 days)



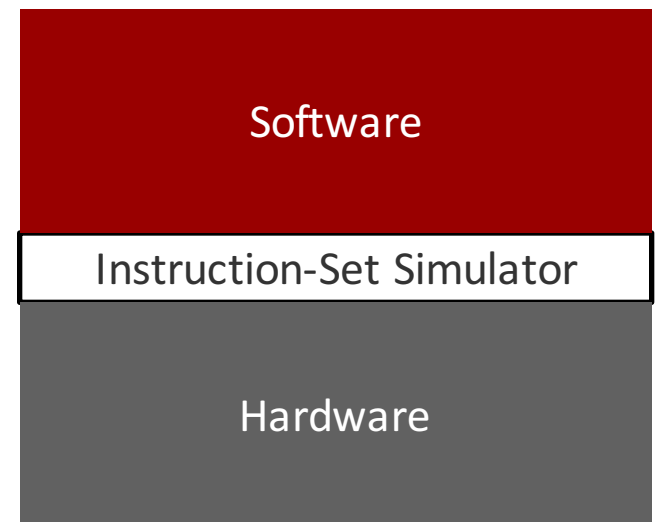
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Interpretive: 1-10 MIPS (1-10 days)

Typical DBT: 100s MIPS (1-3 hours)

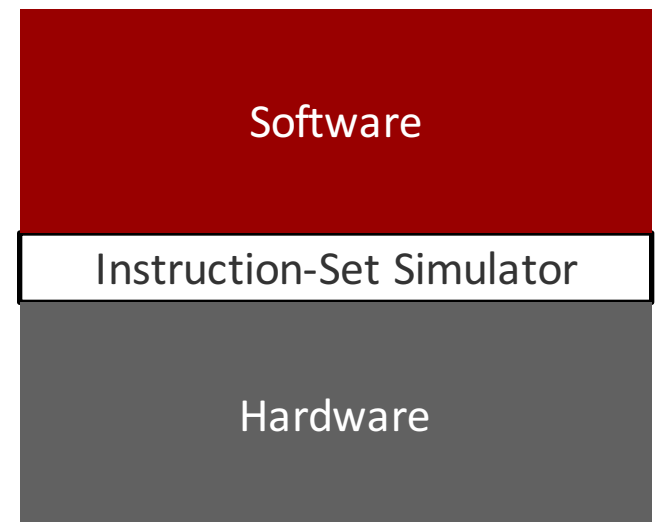


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## Performance

Interpretive: 1-10 MIPS (1-10 days)  
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QEMU DBT: 1000 MIPS (0.5 hours)



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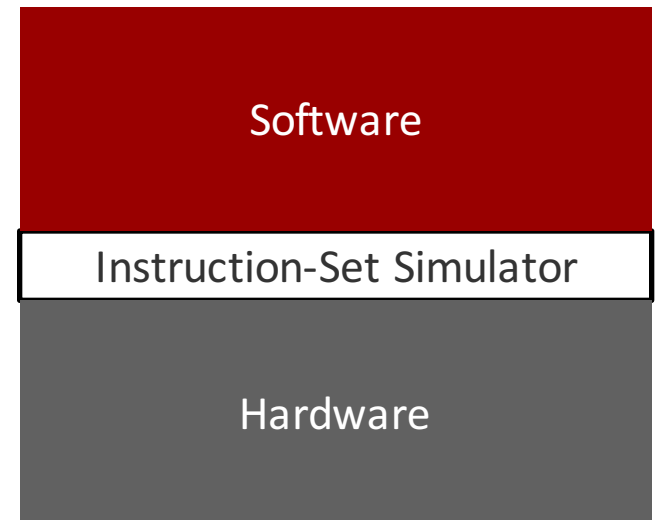
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## Productivity

- Develop
- Extend
- Instrument

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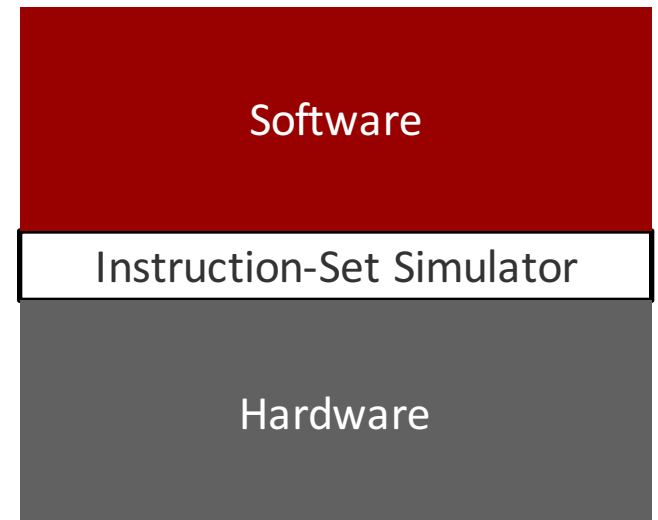
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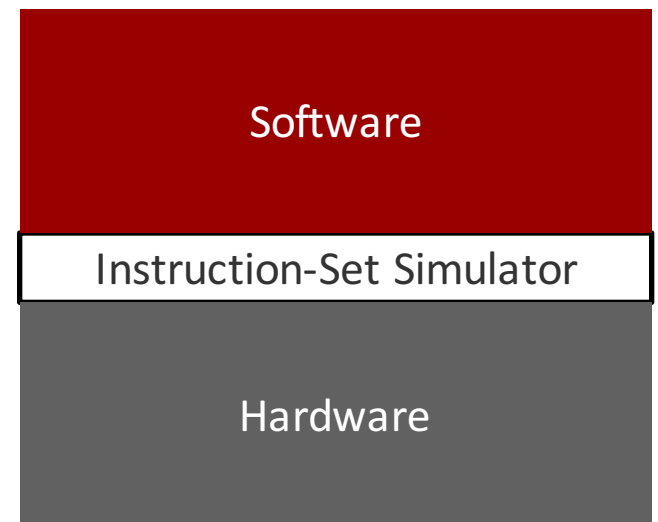
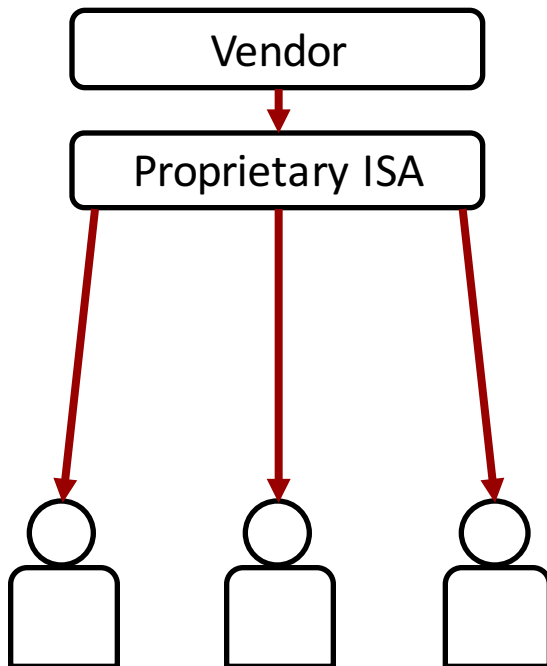
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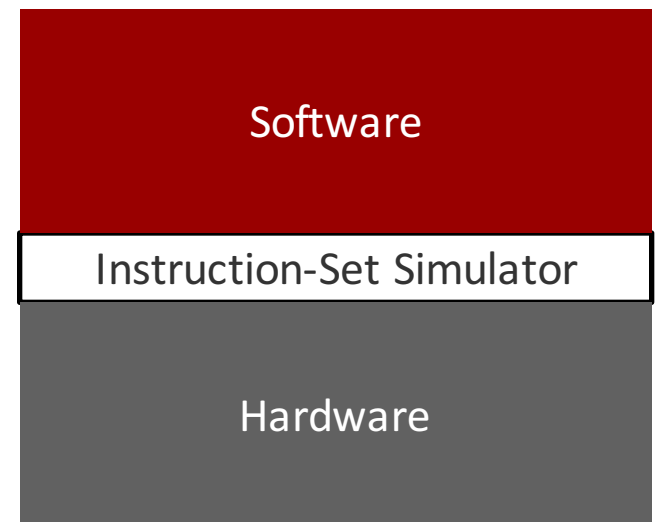
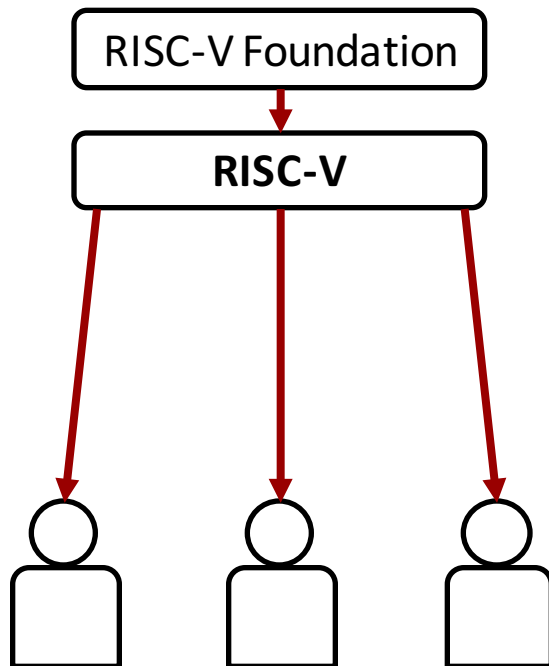
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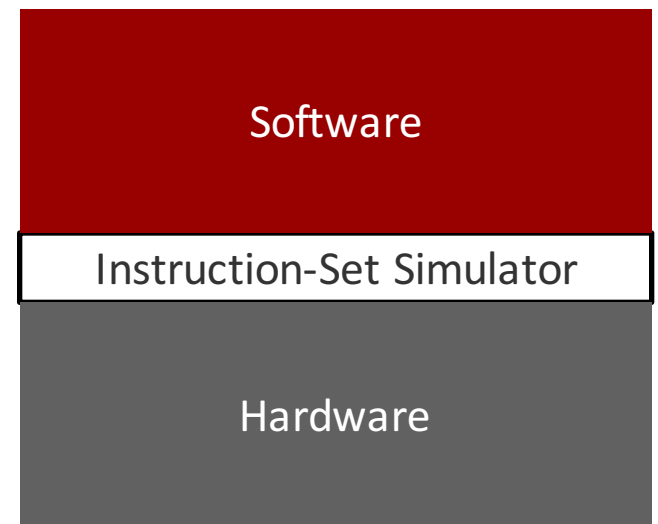
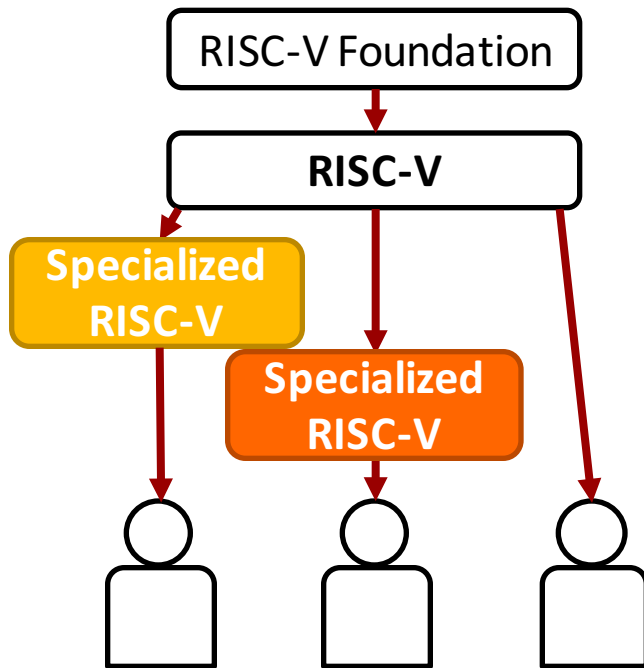
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Productivity



Performance

Productivity



Performance

Architectural  
Description  
Language

Instruction Set  
Interpreter in C  
with DBT

Productivity



Performance

Architectural  
Description  
Language

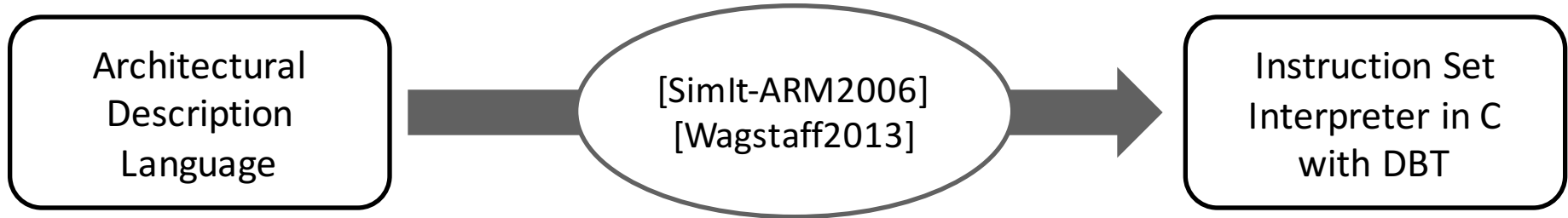


Instruction Set  
Interpreter in C  
with DBT

Productivity



Performance

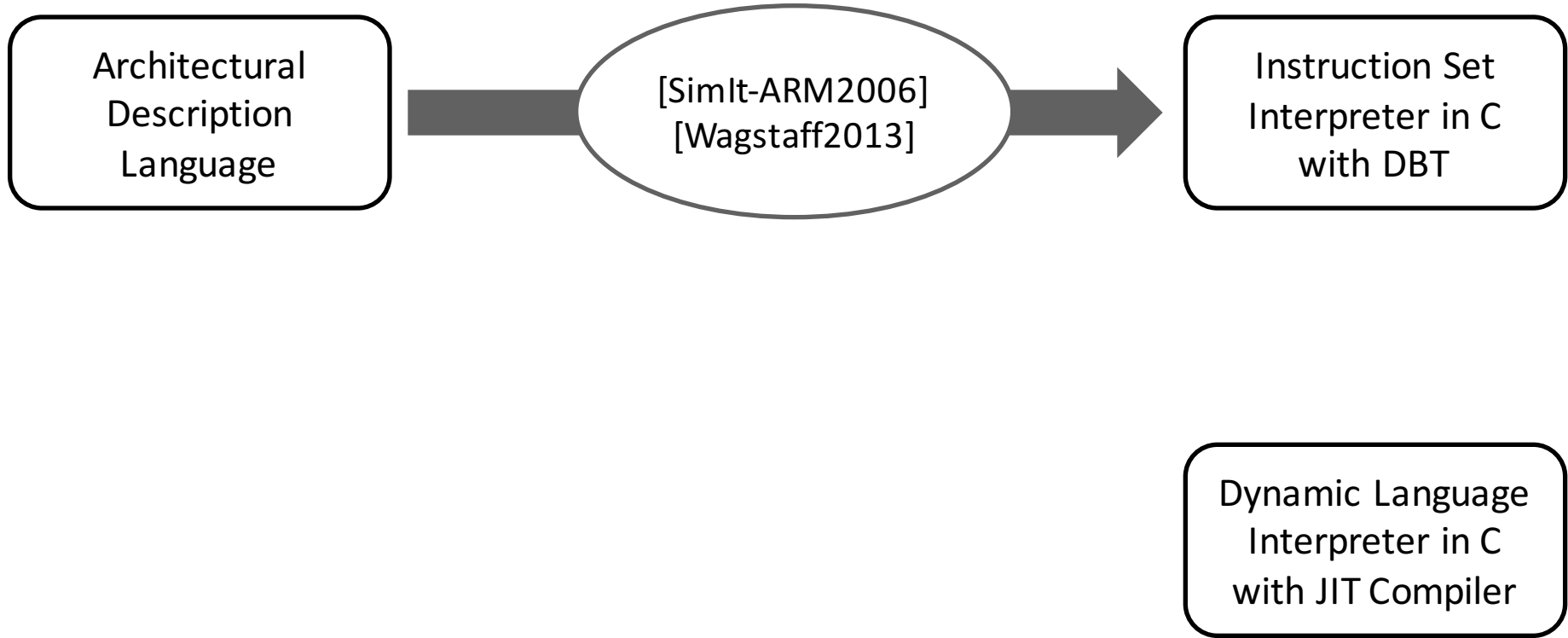


[Simit-ARM2006] J.D’Errico and W.Qin. Constructing Portable Compiled Instruction-Set Simulators — An ADL-Driven Approach. DATE’06.  
[Wagstaff2013] H. Wagstaff, M. Gould, B. Franke, and N.Topham. Early Partial Evaluation in a JIT-Compiled, Retargetable Instruction Set Simulator Generated from a High-Level Architecture Description. DAC’13.

Productivity



Performance



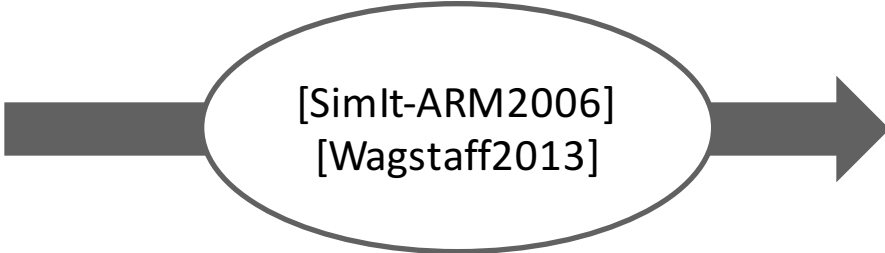


Productivity



Performance

Architectural  
Description  
Language



Instruction Set  
Interpreter in C  
with DBT

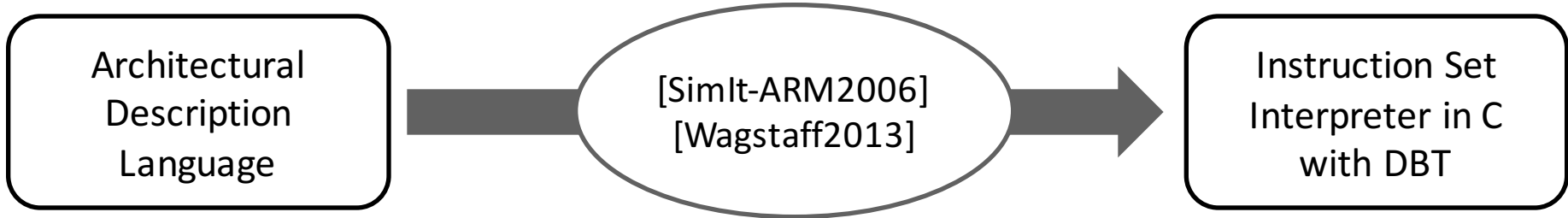
**Key Insight:**  
Similar productivity-performance challenges for building high-performance interpreters of dynamic languages.  
(e.g. JavaScript, Python)

Dynamic Language  
Interpreter in C  
with JIT Compiler

Productivity



Performance



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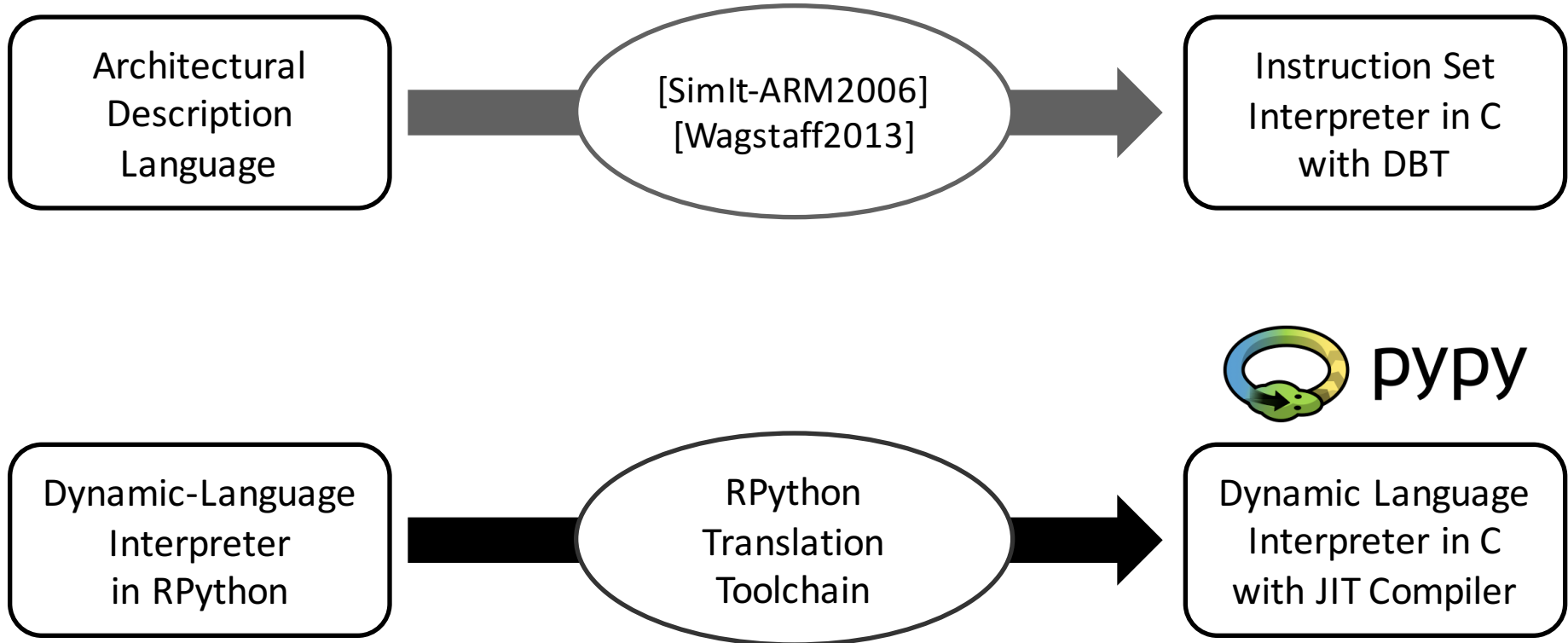


Dynamic Language Interpreter in C with JIT Compiler

Productivity



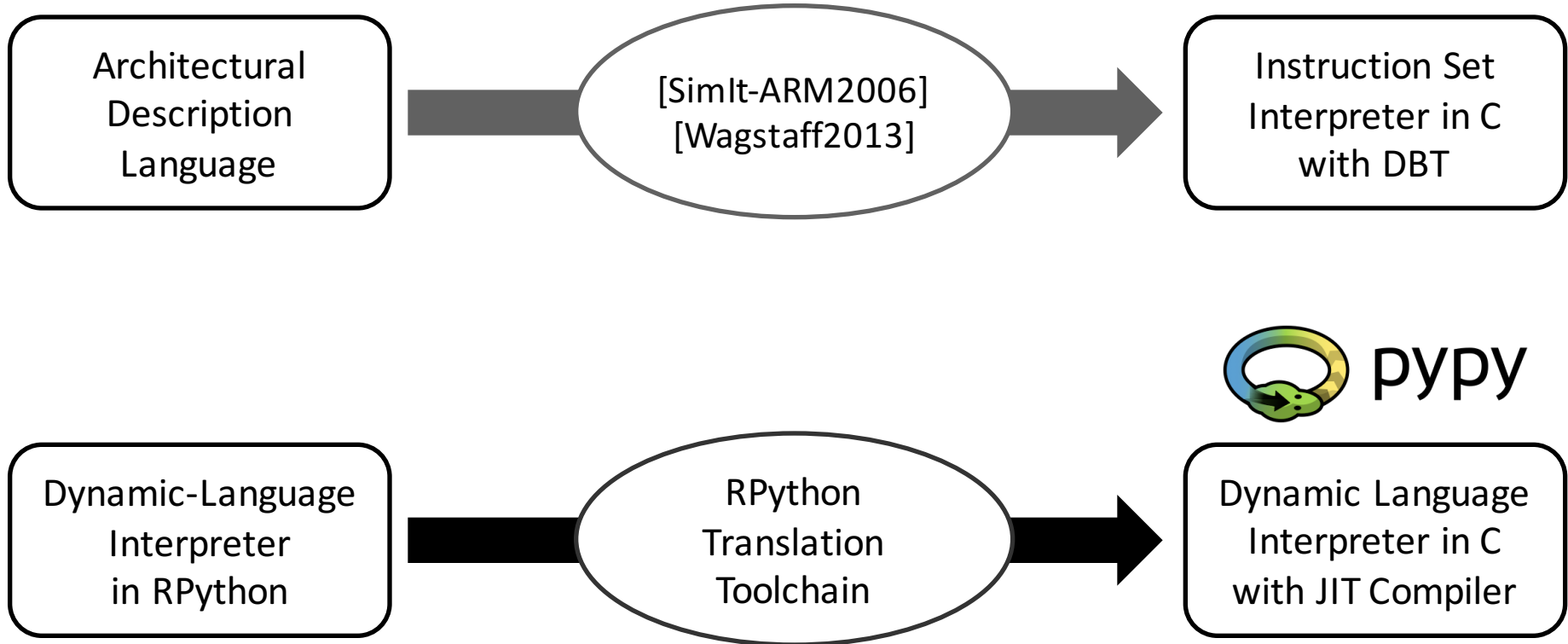
Performance



Productivity



Performance



**Meta-Tracing JIT:  
makes JIT generation generic across languages**

Productivity

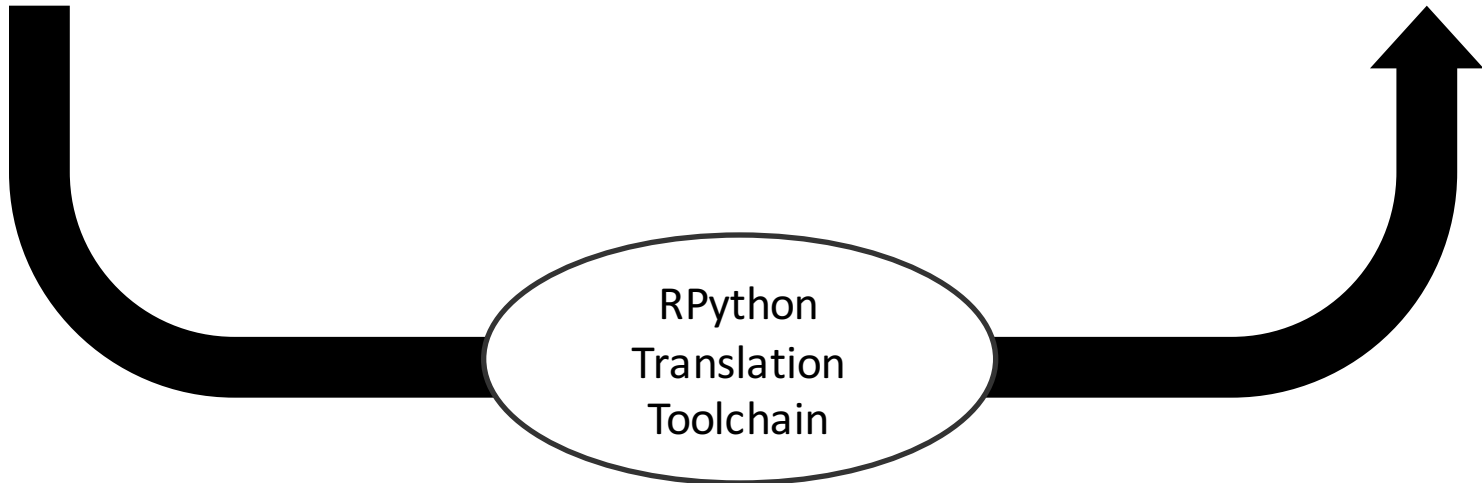


Performance

Architectural  
Description  
Language



Instruction Set  
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with DBT



Productivity

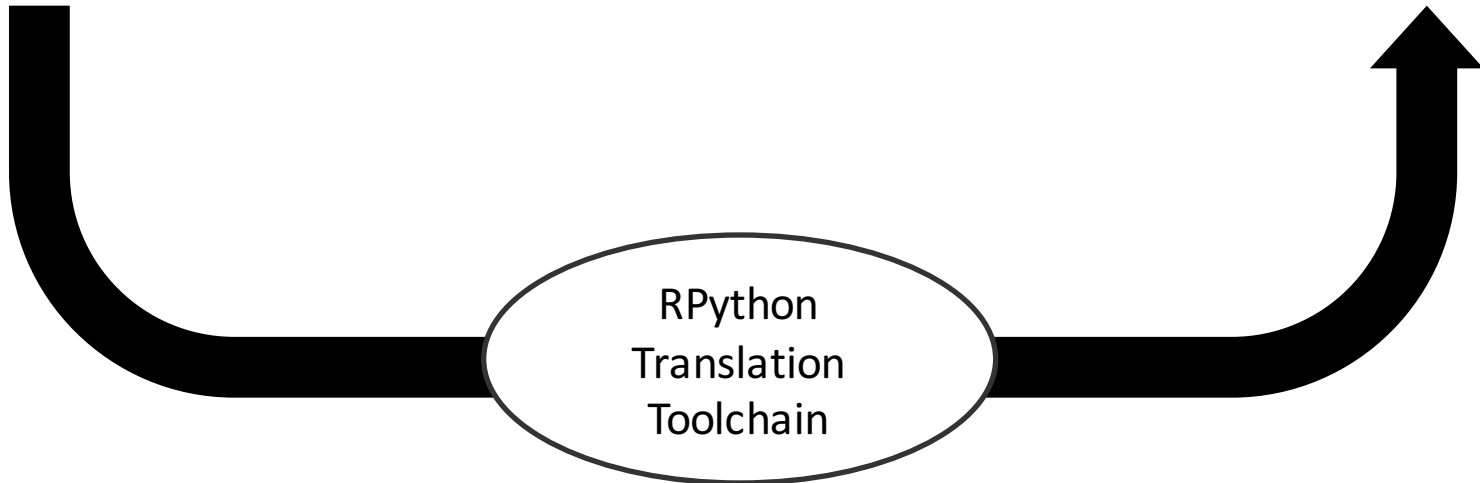


Performance

Architectural  
Description  
Language



Instruction Set  
Interpreter in C  
with DBT



**JIT  $\approx$  DBT**

# Pydgin Architecture Description Language

---

State

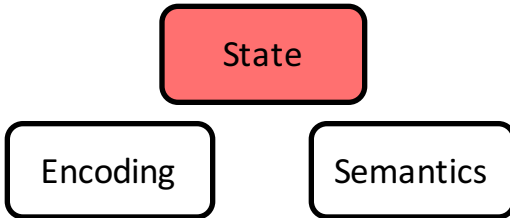
Encoding

Semantics

**Architectural State**  
**Instruction Encoding**  
**Instruction Semantics**

# Pydgin Architecture Description Language

---



## Architectural State

```
class State( object ):
```

```
def __init__( self, memory, reset_addr=0x400 ):
```

```
    self.pc = reset_addr
```

```
    self.rf = RiscVRegisterFile()
```

```
    self.mem = memory
```

```
# optional state if floating point is enabled
```

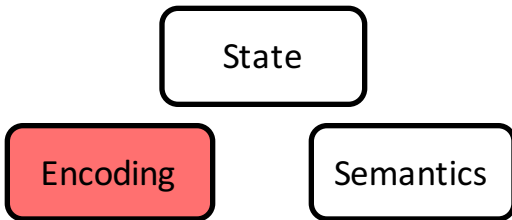
```
if ENABLE_FP:
```

```
    self.fp = RiscVFPRegisterFile()
```

```
    self.fcsr = 0
```



# Pydgin Architecture Description Language



## Instruction Encoding

```
encodings = [  
    # ...  
  
    ['xori', 'xxxxxxxxxxxxxxxxxxxx100xxxxx0010011'],  
    ['ori', 'xxxxxxxxxxxxxxxxxxxx110xxxxx0010011'],  
    ['andi', 'xxxxxxxxxxxxxxxxxxxx111xxxxx0010011'],  
    ['slli', '000000xxxxxxxxxxxx001xxxxx0010011'],  
    ['srli', '000000xxxxxxxxxxxx101xxxxx0010011'],  
    ['srai', '010000xxxxxxxxxxxx101xxxxx0010011'],  
    ['add', '0000000xxxxxxxxxxxx000xxxxx0110011'],  
    ['sub', '0100000xxxxxxxxxxxx000xxxxx0110011'],  
    ['sll', '0000000xxxxxxxxxxxx001xxxxx0110011'],  
  
    # ...  
]
```

# Pydgin Architecture Description Language

---

State

Encoding

Semantics

## Instruction Semantics

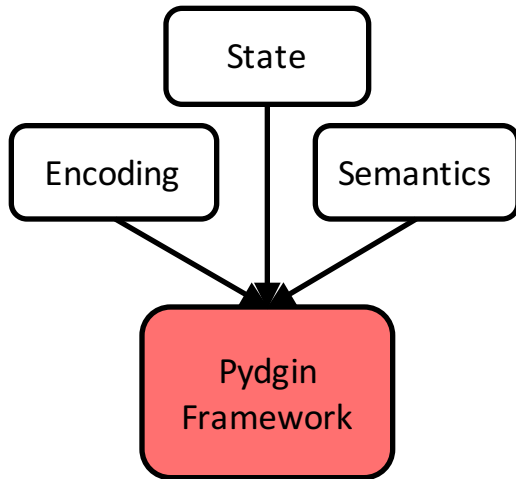
```
def execute_addi( s, inst ):
    s.rf[inst.rd] = s.rf[inst.rs1] + inst.i_imm
    s.pc += 4

def execute_sw( s, inst ):
    addr = trim_xlen( s.rf[inst.rs1] + inst.s_imm )
    s.mem.write( addr, 4, trim_32( s.rf[inst.rs2] ) )
    s.pc += 4

def execute_beq( s, inst ):
    if s.rf[inst.rs1] == s.rf[inst.rs2]:
        s.pc = trim_xlen( s.pc + inst.sb_imm )
    else:
        s.pc += 4
```

# Pydgin Framework

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## Interpreter Loop

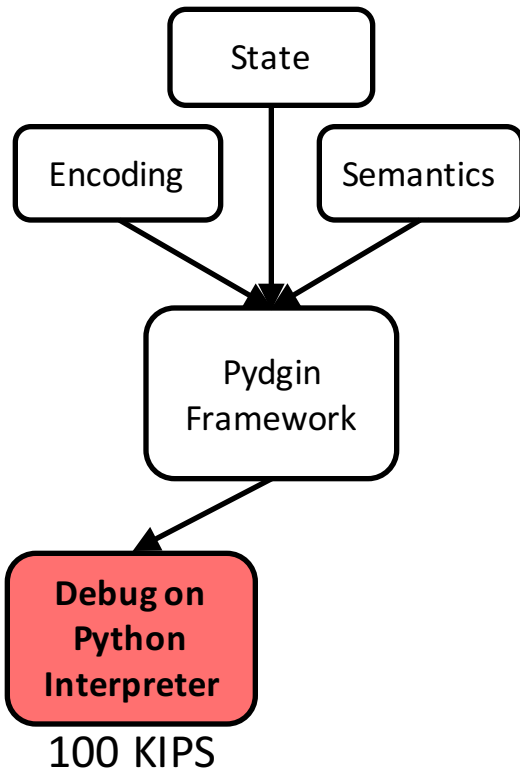
```
def instruction_set_interpreter( memory ):
    state = State( memory )

    while True:

        pc      = state.fetch_pc()

        inst    = memory[ pc ]      # fetch
        execute = decode( inst )   # decode
        execute( state, inst )     # execute
```

# Pydgin Framework



## Interpreter Loop

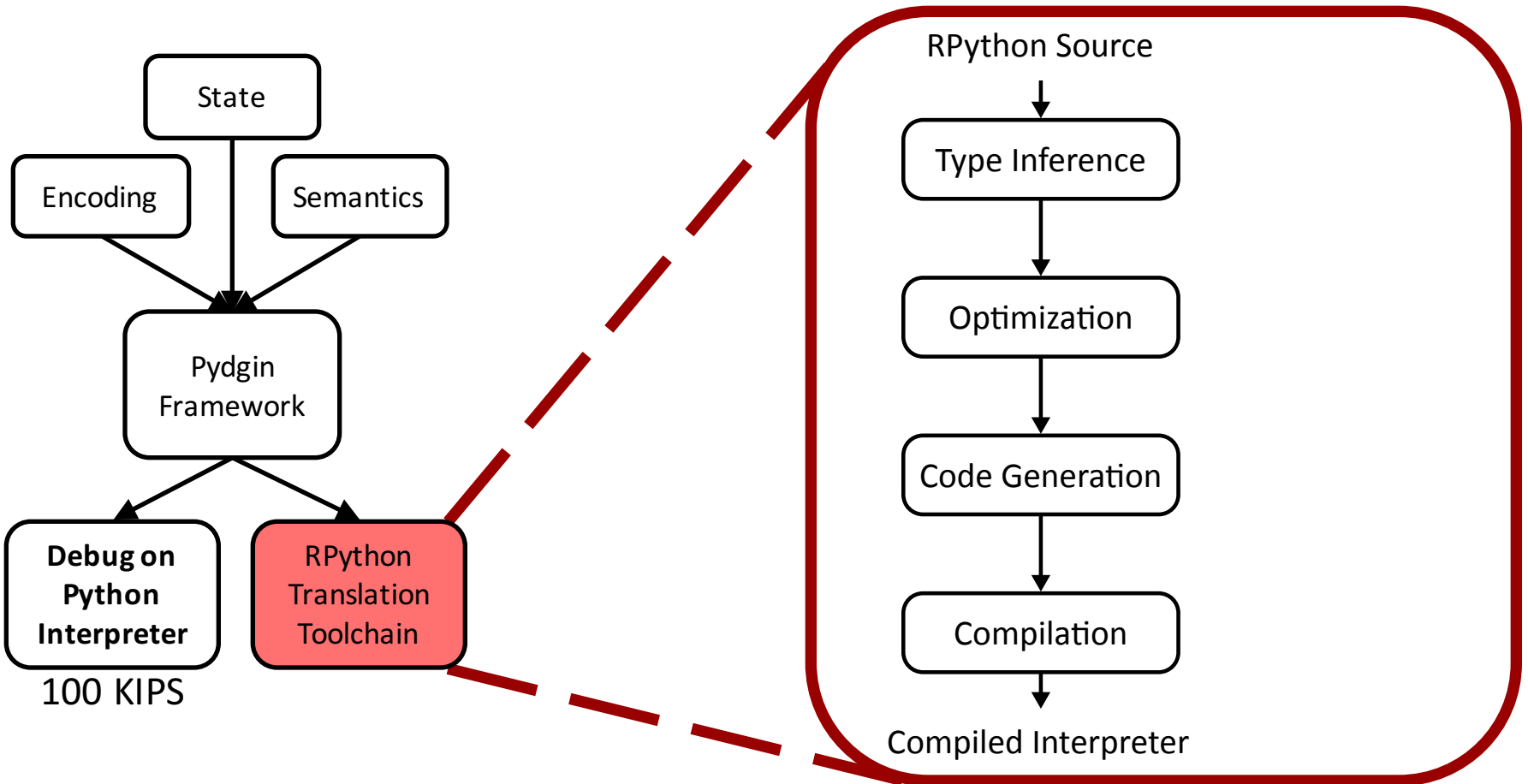
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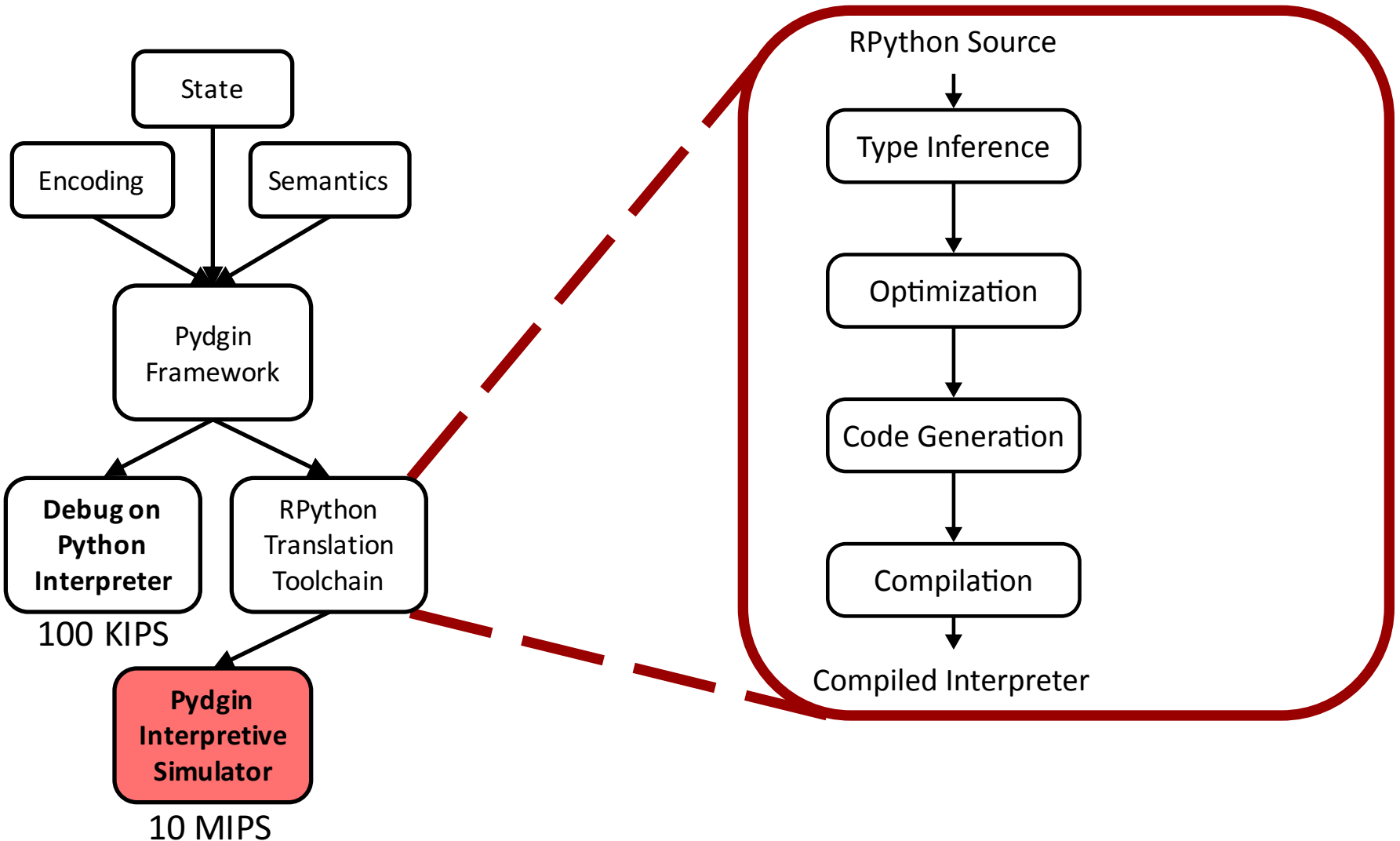
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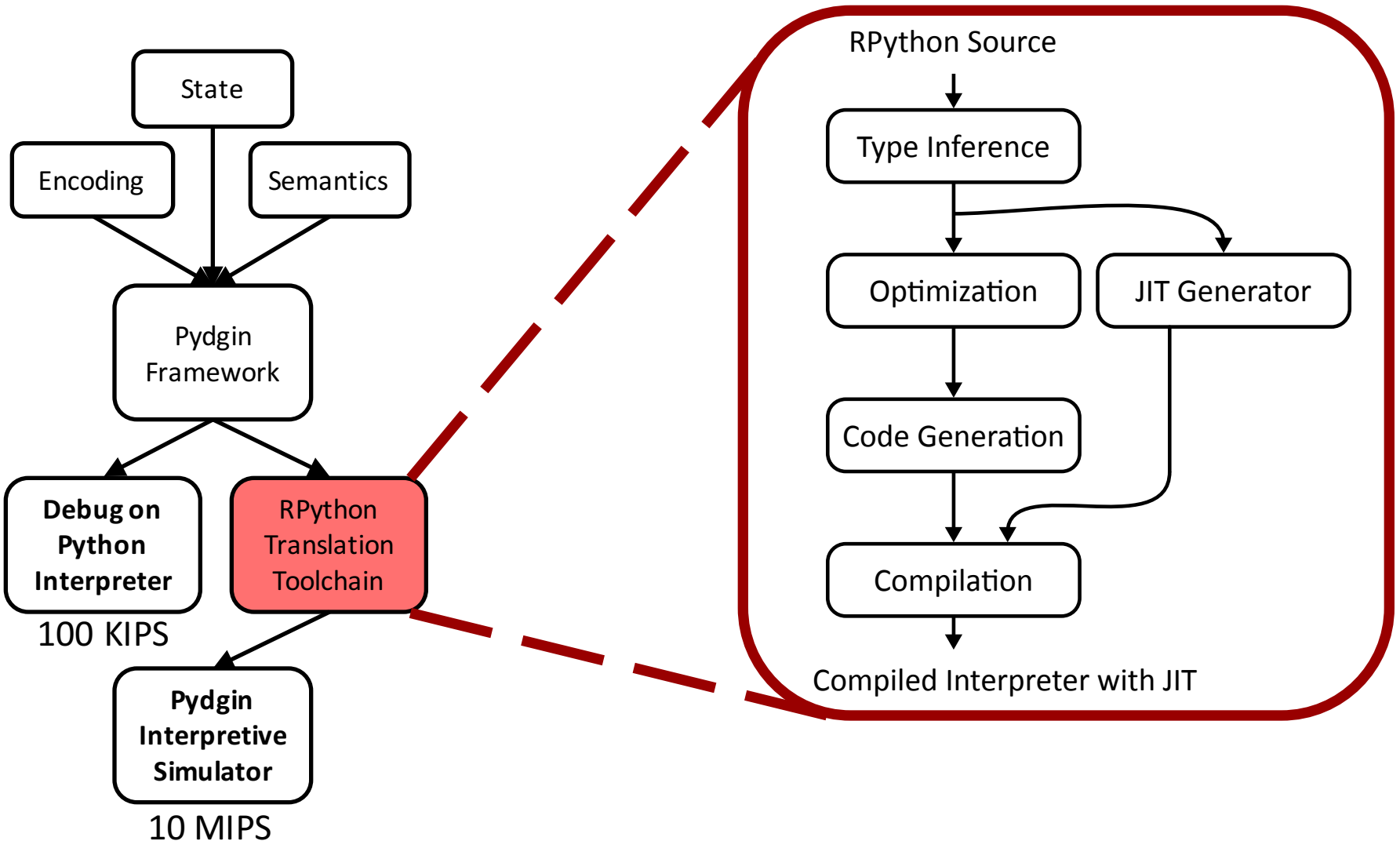
# The RPython Translation Toolchain



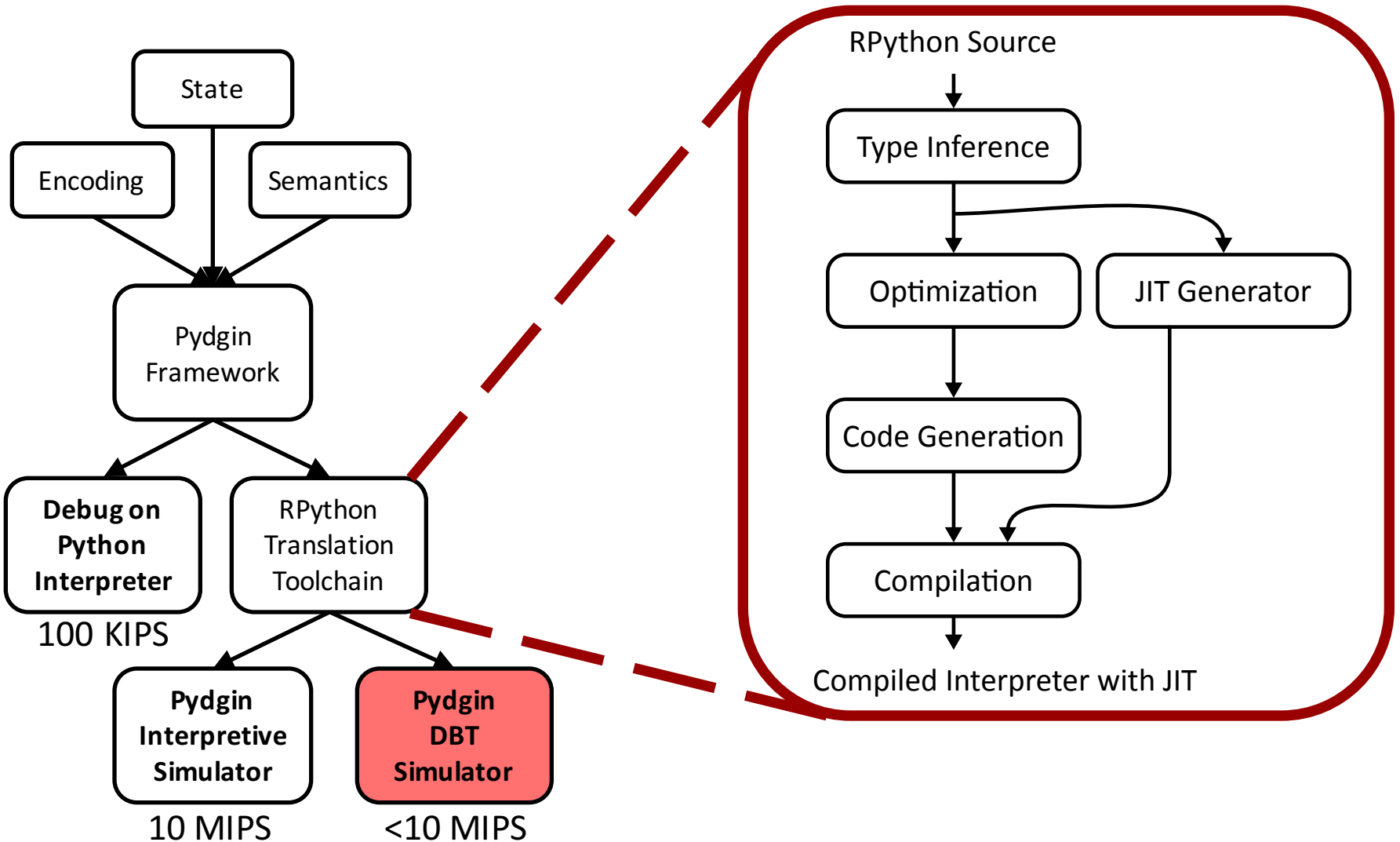
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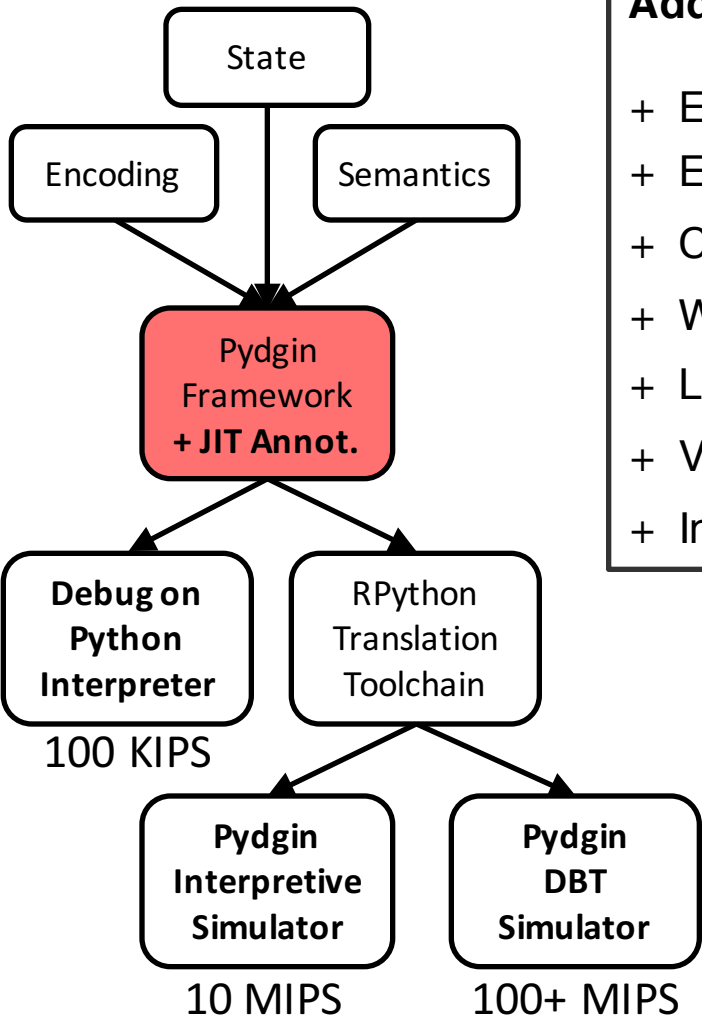


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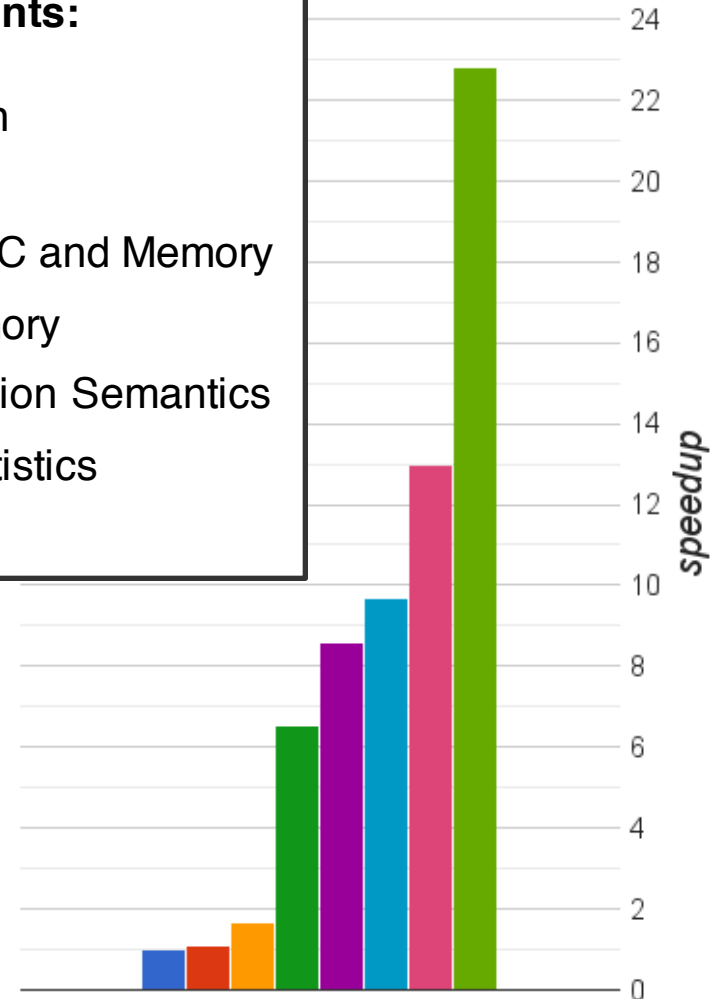


# JIT Annotations and Optimizations



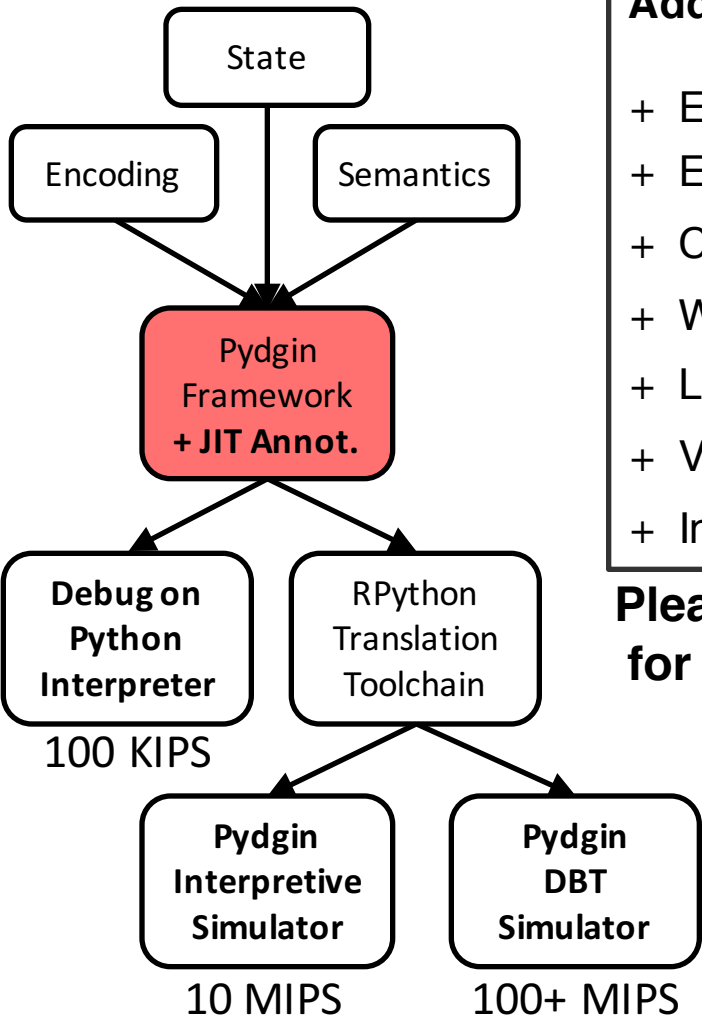
## Additional RPython JIT hints:

- + Elidable Instruction Fetch
- + Elidable Decode
- + Constant Promotion of PC and Memory
- + Word-Based Target Memory
- + Loop Unrolling in Instruction Semantics
- + Virtualizable PC and Statistics
- + Increased Trace Limit



SPECINT206 on ARM

# JIT Annotations and Optimizations

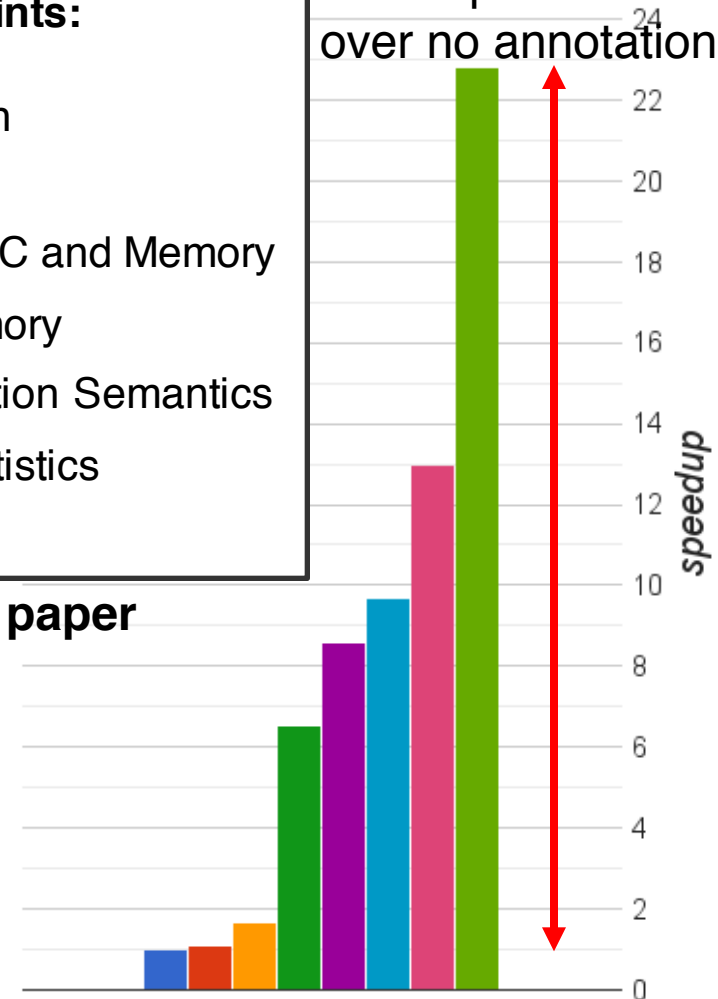


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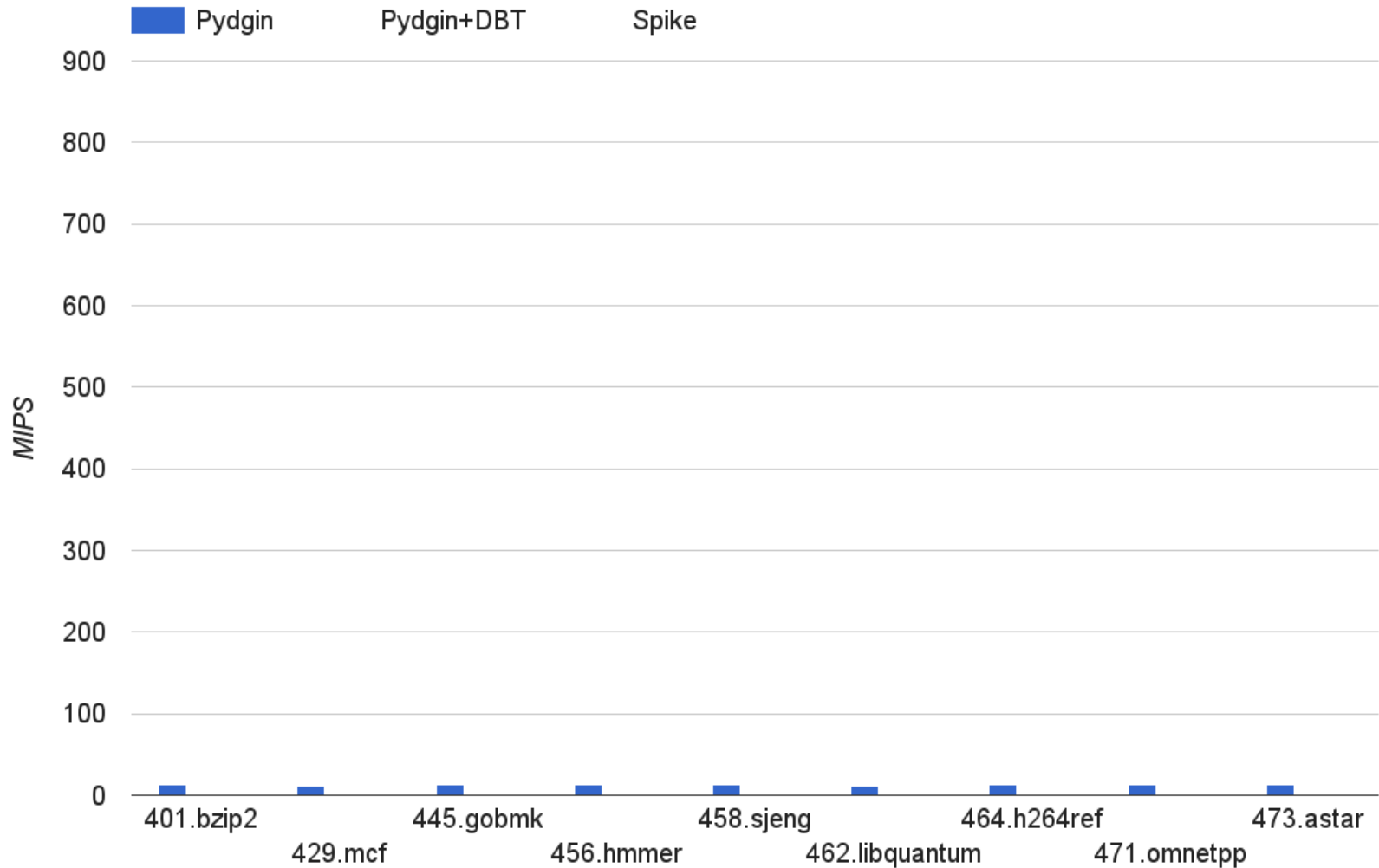
**Please see our ISPASS paper for more details!**

23X improvement over no annotations

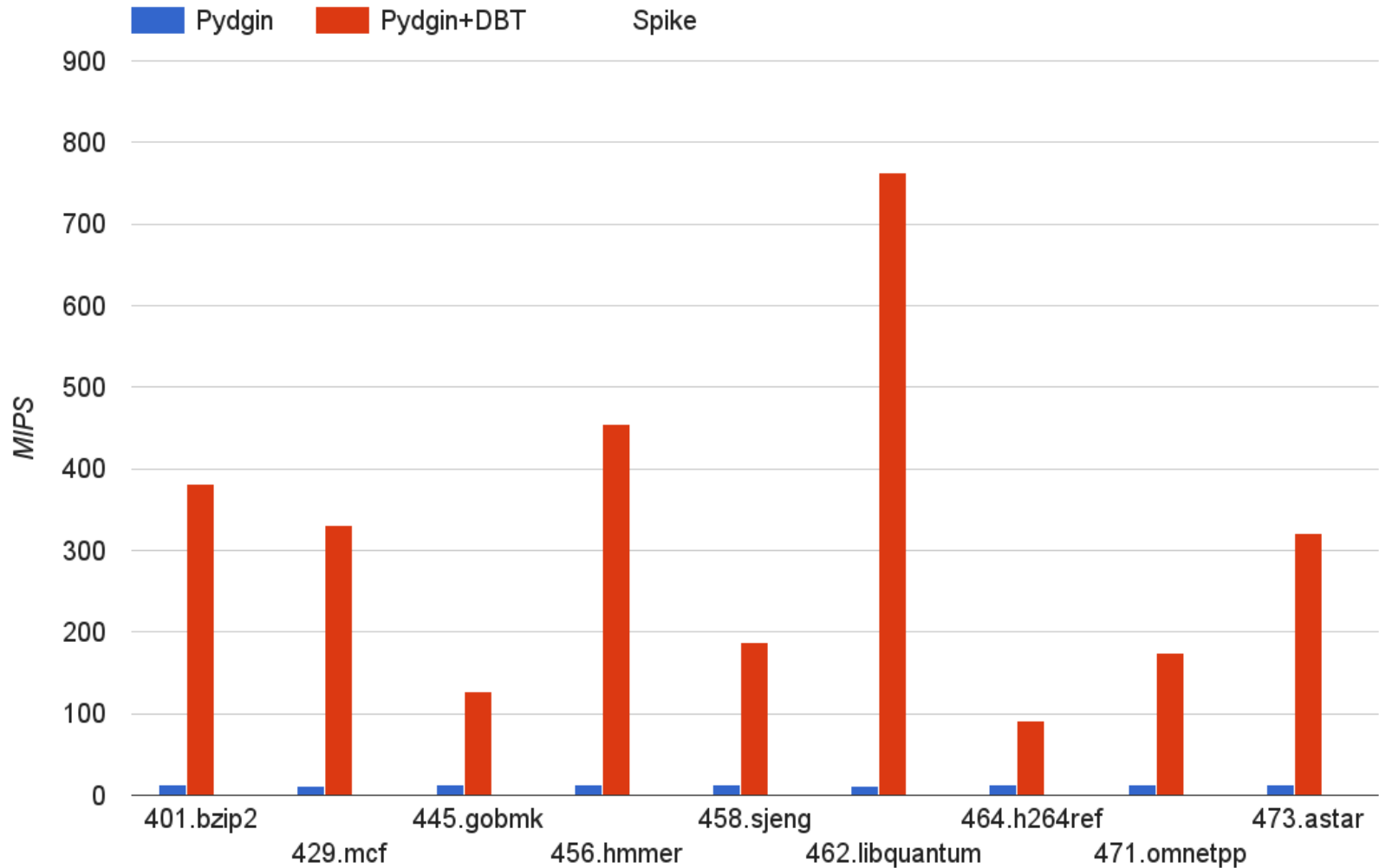


**SPECINT2006 on ARM**

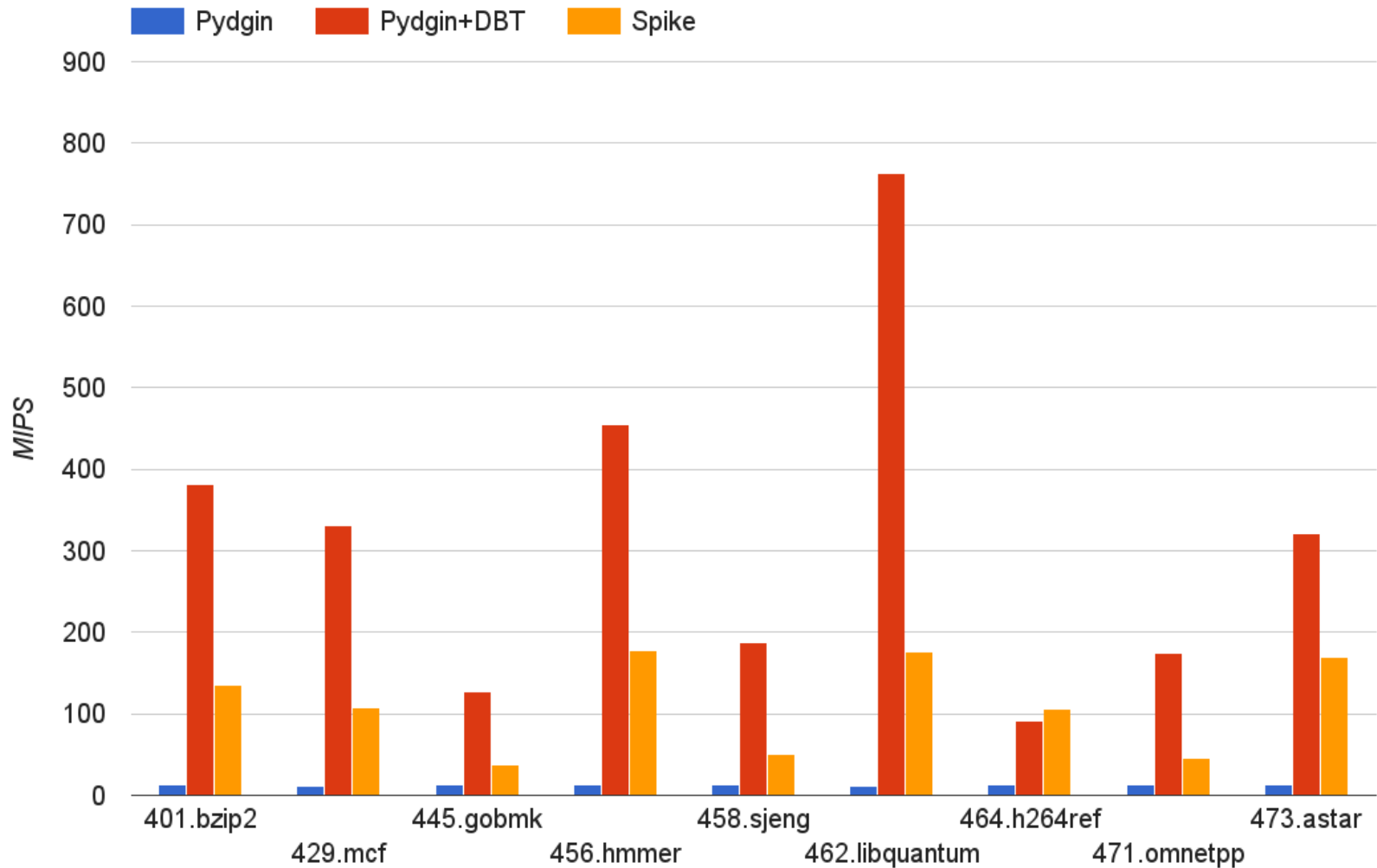
# Pydgin Performance



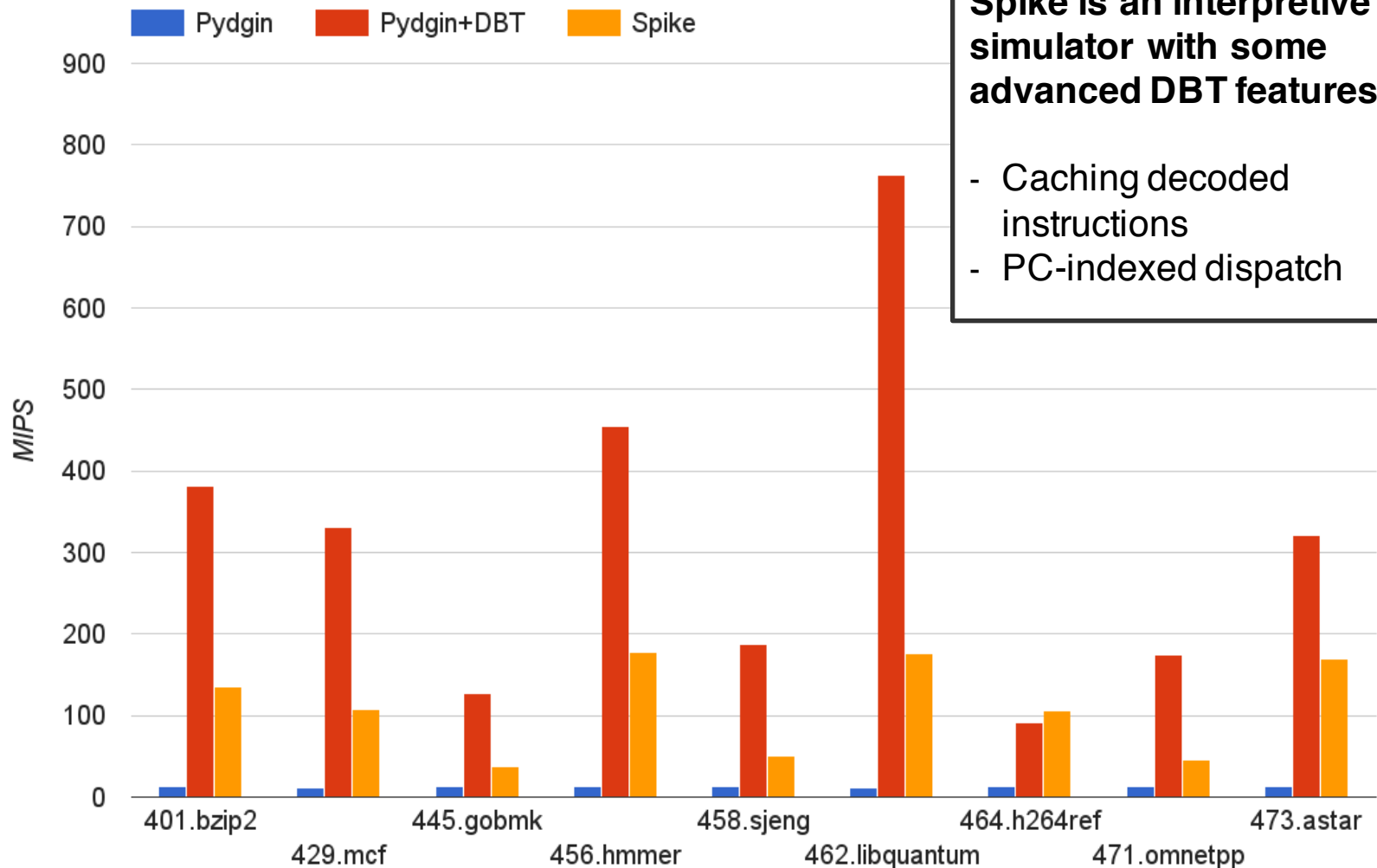
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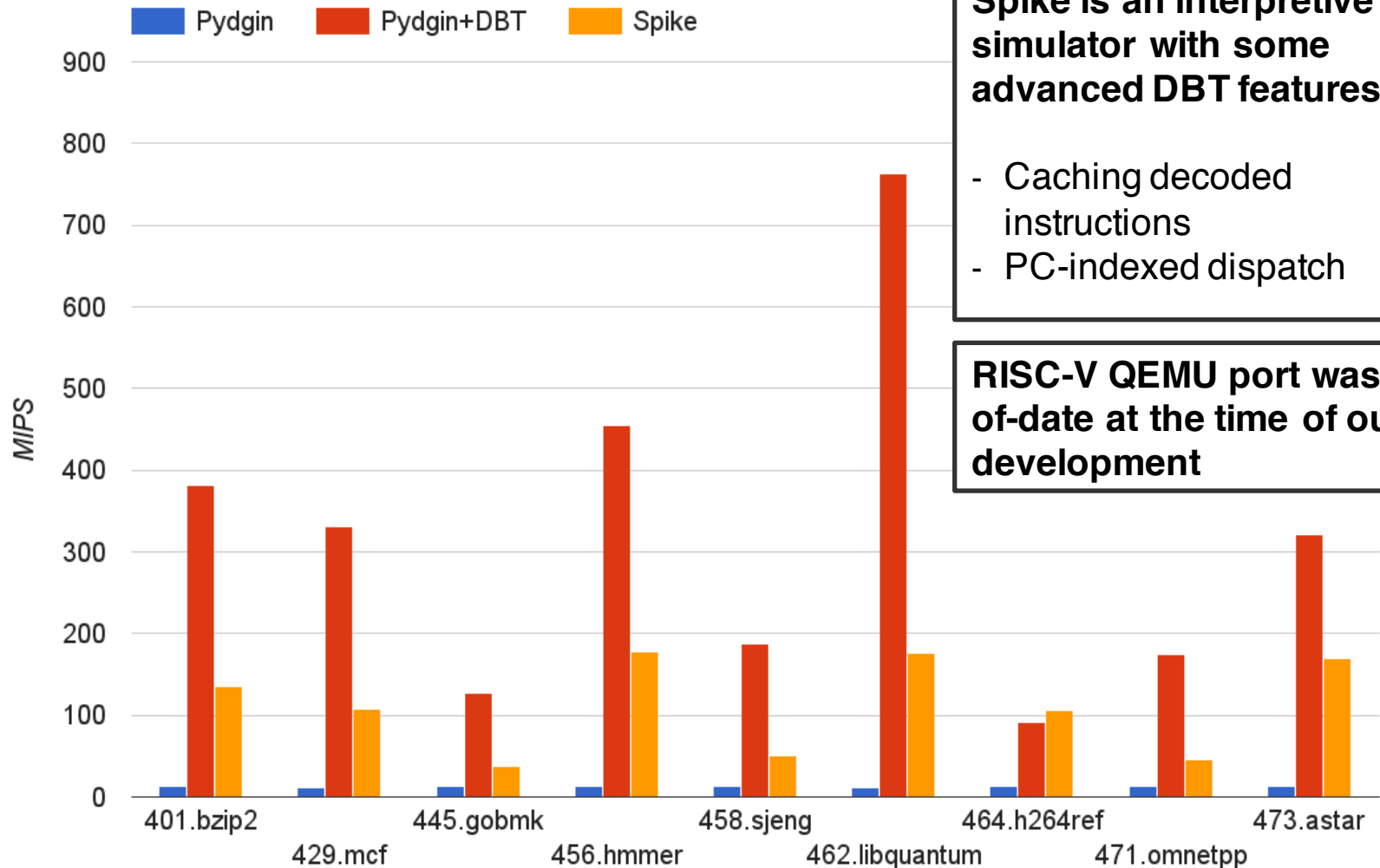
# Pydgin Performance



**Spike is an interpretive simulator with some advanced DBT features:**

- Caching decoded instructions
- PC-indexed dispatch

# Pydgin Performance



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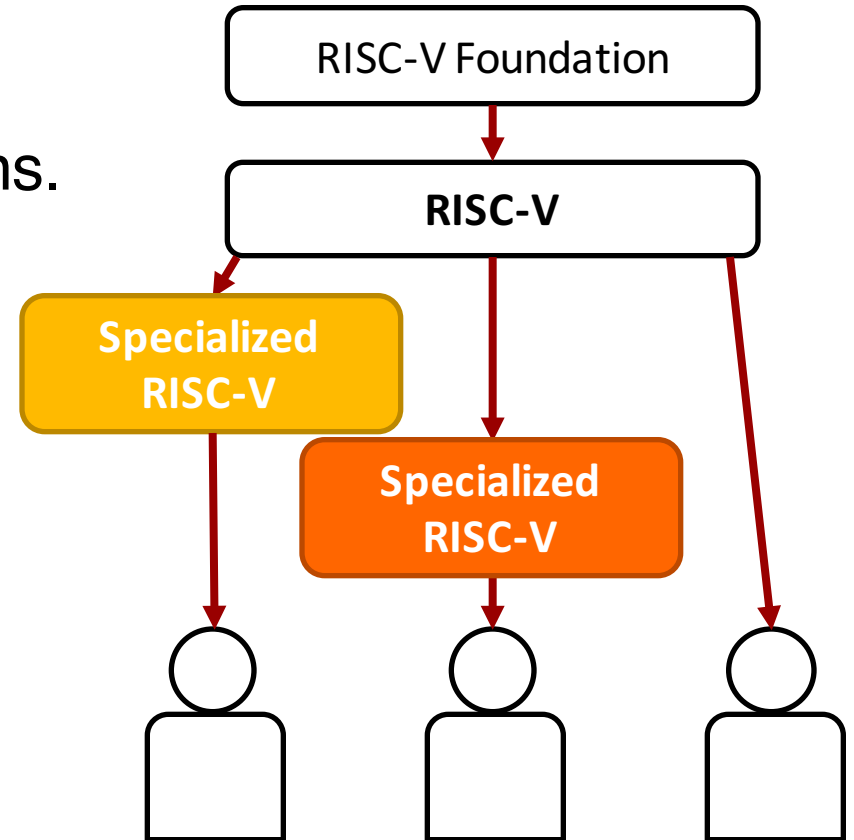
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**RISC-V QEMU port was out-of-date at the time of our development**

# Pydgin Productivity

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RISC-V encourages ISA extensions.



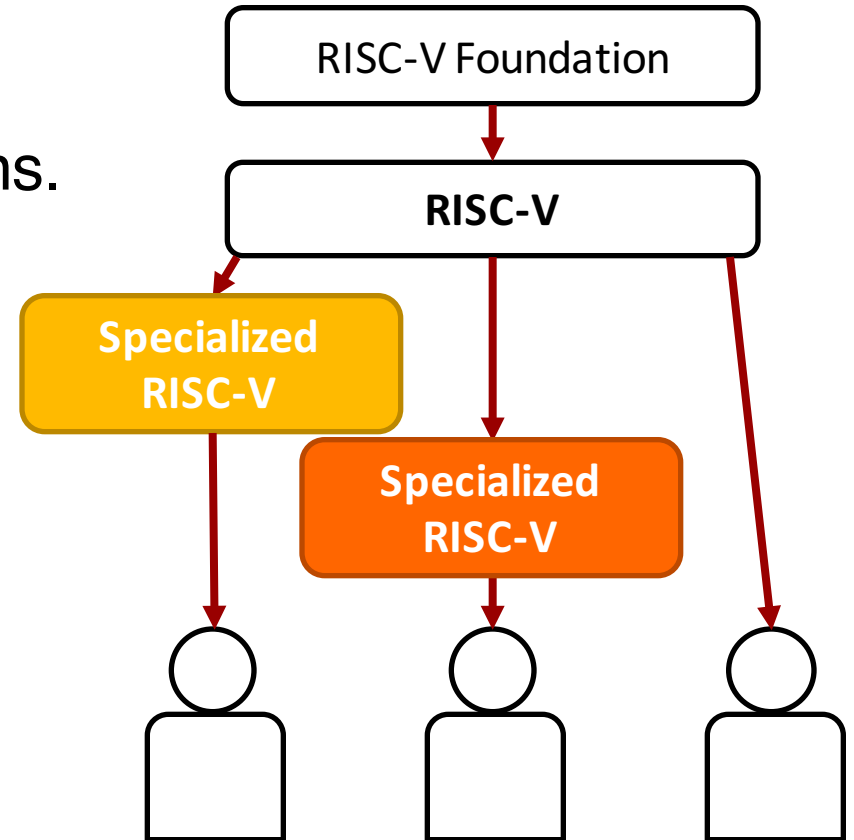


# Pydgin Productivity

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RISC-V encourages ISA extensions.

- Productive Development
- Productive Extensibility
- Productive Instrumentation



# Pydgin RISC-V Development

2015-06-15 Derek Lockhart [riscv] add isa.py skeleton  
2015-06-15 Derek Lockhart [riscv] add riscv-sim.py toplevel  
2015-06-15 Berkin Ibeyi [riscv] add machine.py  
2015-06-15 Derek Lockhart [riscv] ?s to xs, alignment  
2015-06-15 Derek Lockhart [riscv] lowercase inst names, add placeholder funcs  
2015-06-15 Berkin Ibeyi [riscv] first attempt at instruction.py  
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2015-06-15 Berkin Ibeyi [riscv] fix syntax errors, add bootstrap  
2015-06-15 Derek Lockhart [riscv] add xori, ori, xor, or  
2015-06-15 Derek Lockhart [riscv] beq, bne, blt, bge, bltu, bgeu  
2015-06-15 Derek Lockhart [riscv] add hacky, temp impl of csrwr  
2015-06-15 Derek Lockhart [riscv] fix typos in branch insts, hacky impl of jal, jalr  
2015-06-15 Berkin Ibeyi [pydgin] add elf64 reader  
2015-06-15 Berkin Ibeyi [riscv] remove parc junk  
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2015-06-15 Berkin Ibeyi [riscv] add sext\_32  
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2015-06-15 Berkin Ibeyi [riscv] auipc, srl, srai, sll, srl, sra, slliw, srlw, sraiw, sraw  
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2015-06-15 Berkin Ibeyi [riscv] have rf automatically trim the write vals  
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2015-06-17 Derek Lockhart [riscv] fence_i and amov_w instructions
2015-06-17 Berkin Ibeyi [pydgin,parc] add many typing annotations for 32-bit machines
2015-06-17 Berkin Ibeyi [pydgin,pydgin] some more annotations to allow translation w/ debug
2015-06-17 Berkin Ibeyi [pydgin,pydgin] more typing annots for this to work on 64bit
2015-06-17 Berkin Ibeyi [pydgin,parc] make this runnable in interpretive mode
2015-06-17 Berkin Ibeyi [pydgin] more changes to get it working on 64bit
2015-06-17 Berkin Ibeyi [pydgin] clean up comments
2015-06-17 Berkin Ibeyi [riscv] rpython type hacks to get translated
2015-06-17 Berkin Ibeyi [riscv] can run tests on the translated pydgin, beautify test outs
2015-06-17 Berkin Ibeyi [riscv] add gitignore
2015-06-17 Berkin Ibeyi [riscv] more rpython type hacks for trim
2015-06-18 Berkin Ibeyi [riscv] declare virtualizables to keep rpython happy
2015-06-18 Berkin Ibeyi [riscv] do some arith magic to calculate mulh instructions
2015-06-18 Berkin Ibeyi [riscv] some usability improvements to test-all riscv
2015-06-19 Berkin Ibeyi [riscv] bootstrap differently for non-tests
2015-06-19 Derek Lockhart [riscv] add floating-point register file, cleanup Riscv RF init
2015-06-19 Derek Lockhart [riscv] add xlen/flen state, also csr and fcsr reg state
2015-06-19 Berkin Ibeyi [riscv] impl syscall emul wrappers
2015-06-20 Derek Lockhart [riscv] fix type in name of fcsr register
2015-06-20 Derek Lockhart [riscv] implement fp loads, mvs, add/sub/mul using softfloat
2015-06-20 Derek Lockhart [riscv] modify test_all script to support exec from build dir
2015-06-20 Derek Lockhart [riscv] add fclass_s, fclass_d, fmv_d_x insns
2015-06-20 Derek Lockhart [riscv] add fvt_w, fvt_d insns
2015-06-20 Derek Lockhart [riscv] add fvt_w instructions
2015-06-20 Derek Lockhart [softfloat] add missing .h files, oops
2015-06-20 Derek Lockhart [riscv] fix bugs in fp condition flags, flw
2015-06-20 Berkin Ibeyi [riscv] ignore fst, fld insns
2015-06-20 Berkin Ibeyi [riscv] override default stat struct with riscv-specific struct
2015-06-20 Berkin Ibeyi [riscv] add regmap
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2015-06-20 Derek Lockhart [riscv] fix type in name of fcsr register
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2015-06-20 Derek Lockhart [riscv] modify test-all script to support exec from build dir
2015-06-20 Derek Lockhart [riscv] add f(class_s, f(class_d, fmv_d_x insns
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# Pydgin RISC-V Development

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2015-06-16 Berkin Ibeyi [riscv] impl ld, sd
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2015-06-20 Derek Lockhart [riscv] implement fp loads, mvs, add/sub/mul using sofffloat
2015-06-20 Derek Lockhart [riscv] modify test-all script to support exec from build dir
2015-06-20 Derek Lockhart [riscv] add f(class_s, f(class_d, fmv_d_x insns
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2015-06-20 Berkin Ibeyi [riscv] revert "riscv: hack in machine to get translated"
2015-06-20 Derek Lockhart [riscv] add fcvt_w instructions (details)
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2015-06-21 Berkin Ibeyi [riscv] fix ld/st/jump bugs that show up in dense mem
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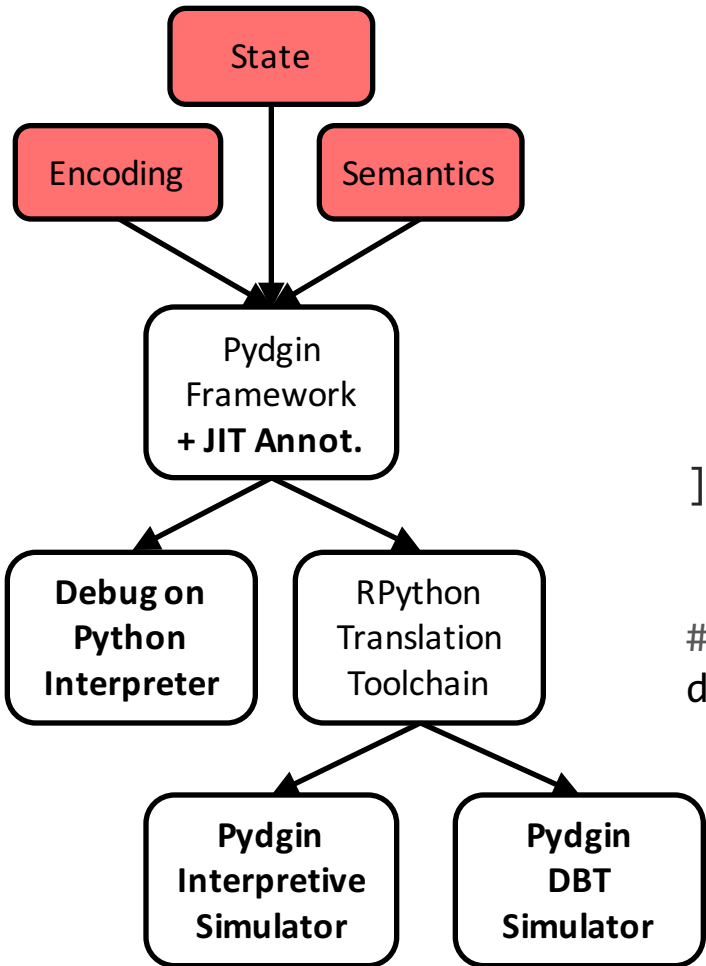
# Pydgin RISC-V Development

**100+ MIPS simulator  
after 9 days of development!**

```
2013-06-15 Derek Lockhart [riscv] add isa.py skeleton
2013-06-15 Derek Lockhart [riscv] add riscv-sim.py toplevel
2013-06-15 Berkin Ibeyi [riscv] add machine.py
2013-06-15 Derek Lockhart [riscv] %s to %s, alignment
2013-06-15 Derek Lockhart [riscv] lowercase inst names, add placeholder funcs
2013-06-15 Derek Lockhart [riscv] first attempt at instruction.py
2013-06-15 Derek Lockhart [riscv] add helpers.py, some hacky inst impls
2013-06-15 Derek Lockhart [riscv] addw inst
2013-06-15 Berkin Ibeyi [riscv] fix syntax errors, add bootstrap
2013-06-15 Derek Lockhart [riscv] add mori, ori, nor, or
2013-06-15 Derek Lockhart [riscv] beq, bne, blt, bge, bltu, bgeu
2013-06-15 Derek Lockhart [riscv] add hacky, temp impl of csrwr
2013-06-15 Derek Lockhart [riscv] fix typos in branch insts, hacky impl of jal, jalr
2013-06-15 Berkin Ibeyi [pydgin] add elf64 reader
2013-06-15 Berkin Ibeyi [riscv] remove parc junk
2013-06-15 Berkin Ibeyi [riscv] fix reset vector
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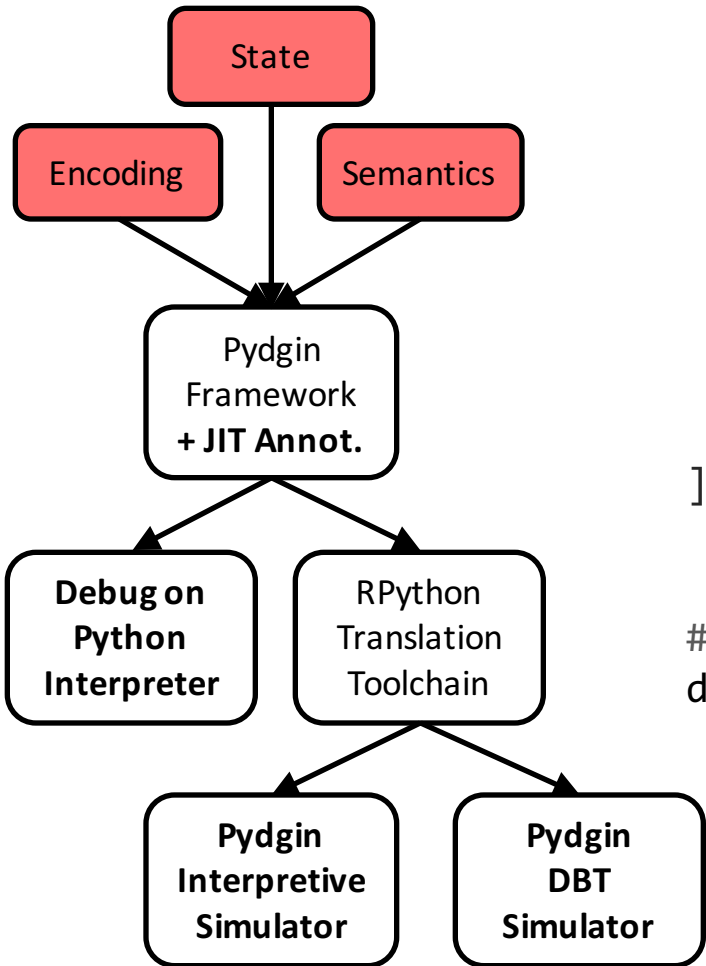
# Pydgin Extensibility



```
encodings = [  
    # ...  
    ['andi',      'xxxxxxxxxxxxxxxxxxxx111xxxxx0010011'],  
    ['slli',      '000000xxxxxxxxxxxx001xxxxx0010011'],  
    ['srli',      '000000xxxxxxxxxxxx101xxxxx0010011'],  
    ['srai',      '010000xxxxxxxxxxxx101xxxxx0010011'],  
    ['add',       '0000000xxxxxxxxxxxx000xxxxx0110011'],  
    # ...  
    ['custom2',  'xxxxxxxxxxxxxxxxxxxx000xxxxx1011011'],  
    # ...  
]
```

```
# greatest common divisor semantics  
def execute_gcd( s, inst ):
```

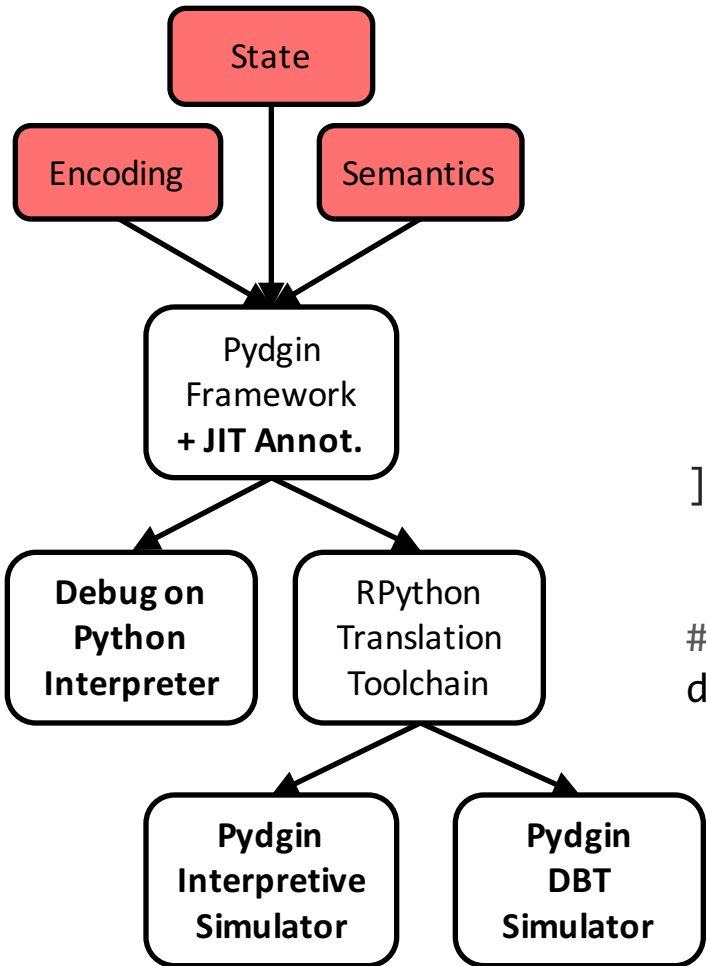
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    ['add',       '0000000xxxxxxxxxxxxx000xxxxx0110011'],  
    # ...  
    ['gcd',       'xxxxxxxxxxxxxxxxxxxx000xxxxx1011011'],  
    # ...  
]
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```
# greatest common divisor semantics  
def execute_gcd( s, inst ):
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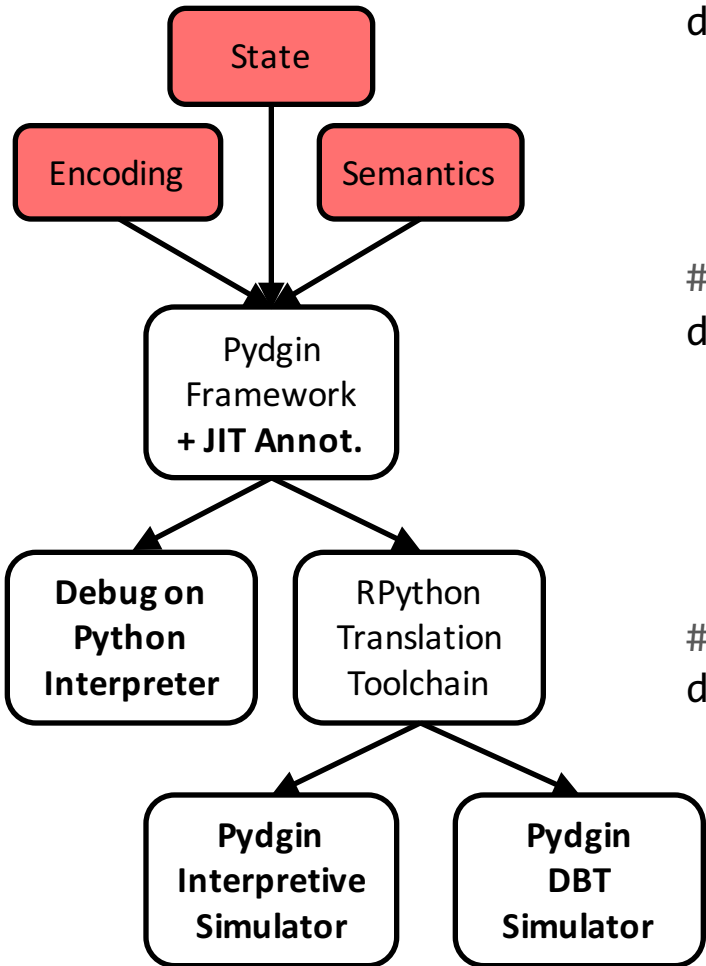
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    ['add',       '0000000xxxxxxxxxxxxx000xxxxx0110011'],  
    # ...  
    ['gcd',       'xxxxxxxxxxxxxxxxxxxx000xxxxx1011011'],  
    # ...  
]
```

```
# greatest common divisor semantics  
def execute_gcd( s, inst ):  
    a, b = s.rf[inst.rs1], s.rf[inst.rs2]  
    while b:  
        a, b = b, a%b  
        s.rf[inst.rd] = a  
        s.pc += 4
```

# Pydgin Instrumentation



```
# count number of adds
def execute_addi( s, inst ):
    s.rf[inst.rd] = s.rf[inst.rs1] + inst.i_imm

    s.pc += 4

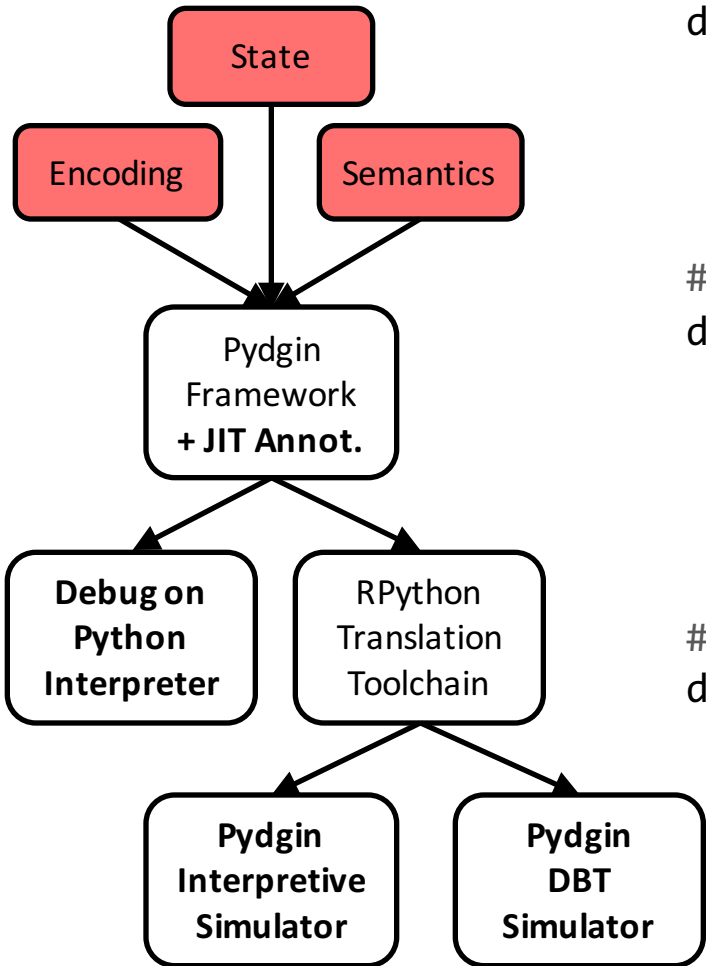
# count misaligned stores
def execute_sw( s, inst ):
    addr = trim_xlen( s.rf[inst.rs1] + inst.s_imm )

    s.mem.write( addr, 4, trim_32( s.rf[inst.rs2] ) )
    s.pc += 4

# record and count all executed loops
def execute_beq( s, inst ):
    if s.rf[inst.rs1] == s.rf[inst.rs2]:

        s.pc = trim_xlen( s.pc + inst.sb_imm )
    else:
        s.pc += 4
```

# Pydgin Instrumentation



```
# count number of adds
def execute_addi( s, inst ):
    s.rf[inst.rd] = s.rf[inst.rs1] + inst.i_imm
    s.num_adds += 1
    s.pc += 4

# count misaligned stores
def execute_sw( s, inst ):
    addr = trim_xlen( s.rf[inst.rs1] + inst.s_imm )

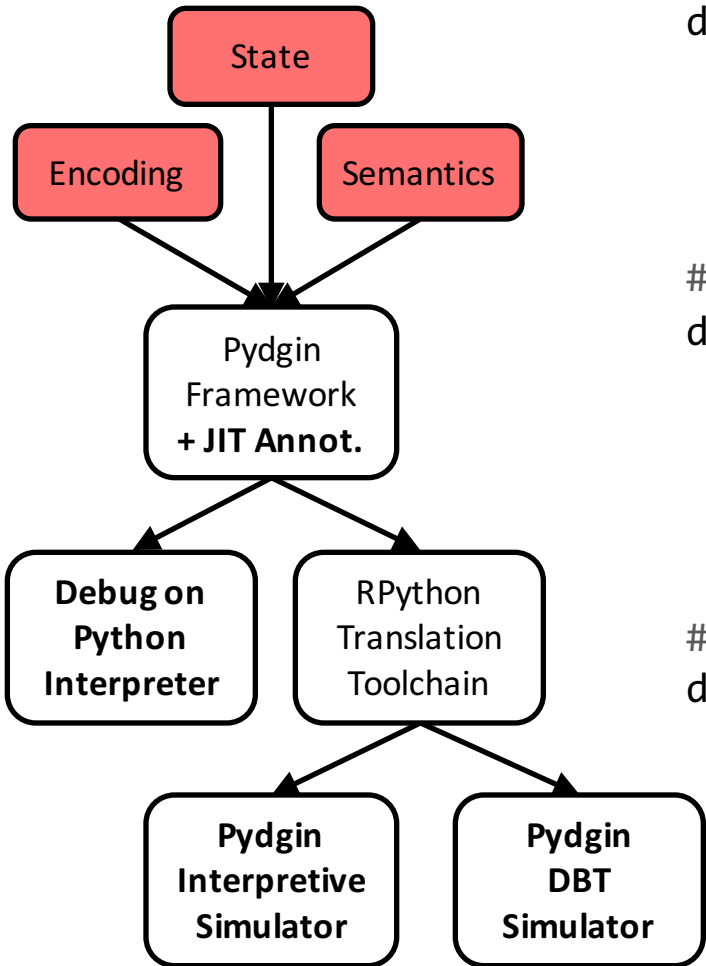
    s.mem.write( addr, 4, trim_32( s.rf[inst.rs2] ) )
    s.pc += 4

# record and count all executed loops
def execute_beq( s, inst ):
    if s.rf[inst.rs1] == s.rf[inst.rs2]:

        s.pc = trim_xlen( s.pc + inst.sb_imm )
    else:
        s.pc += 4
```



# Pydgin Instrumentation

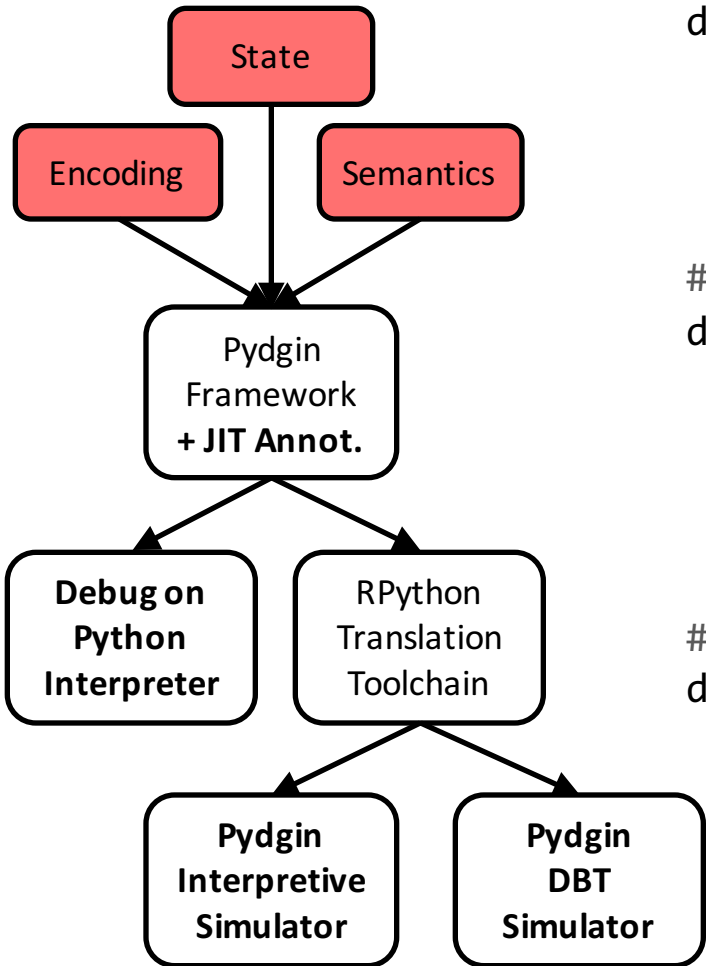


```
# count number of adds
def execute_addi( s, inst ):
    s.rf[inst.rd] = s.rf[inst.rs1] + inst.i_imm
    s.num_adds += 1
    s.pc += 4

# count misaligned stores
def execute_sw( s, inst ):
    addr = trim_xlen( s.rf[inst.rs1] + inst.s_imm )
    if addr % 4 != 0: s.num_misaligned += 1
    s.mem.write( addr, 4, trim_32( s.rf[inst.rs2] ) )
    s.pc += 4

# record and count all executed loops
def execute_beq( s, inst ):
    if s.rf[inst.rs1] == s.rf[inst.rs2]:
        s.pc = trim_xlen( s.pc + inst.sb_imm )
    else:
        s.pc += 4
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# Pydgin Instrumentation



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# count number of adds
def execute_addi( s, inst ):
    s.rf[inst.rd] = s.rf[inst.rs1] + inst.i_imm
    s.num_adds += 1
    s.pc += 4

# count misaligned stores
def execute_sw( s, inst ):
    addr = trim_xlen( s.rf[inst.rs1] + inst.s_imm )
    if addr % 4 != 0: s.num_misaligned += 1
    s.mem.write( addr, 4, trim_32( s.rf[inst.rs2] ) )
    s.pc += 4

# record and count all executed loops
def execute_beq( s, inst ):
    if s.rf[inst.rs1] == s.rf[inst.rs2]:
        old_pc = s.pc
        s.pc = trim_xlen( s.pc + inst.sb_imm )
        if s.pc <= old_pc: s.loops[(s.pc, old_pc)] += 1
    else:
        s.pc += 4
```

# Pydgin in Our Research Group

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- Statistics for software-defined regions

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- Statistics for software-defined regions
- Data-structure specialization experimentation

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- Statistics for software-defined regions
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- Control- and memory-divergence for SIMD

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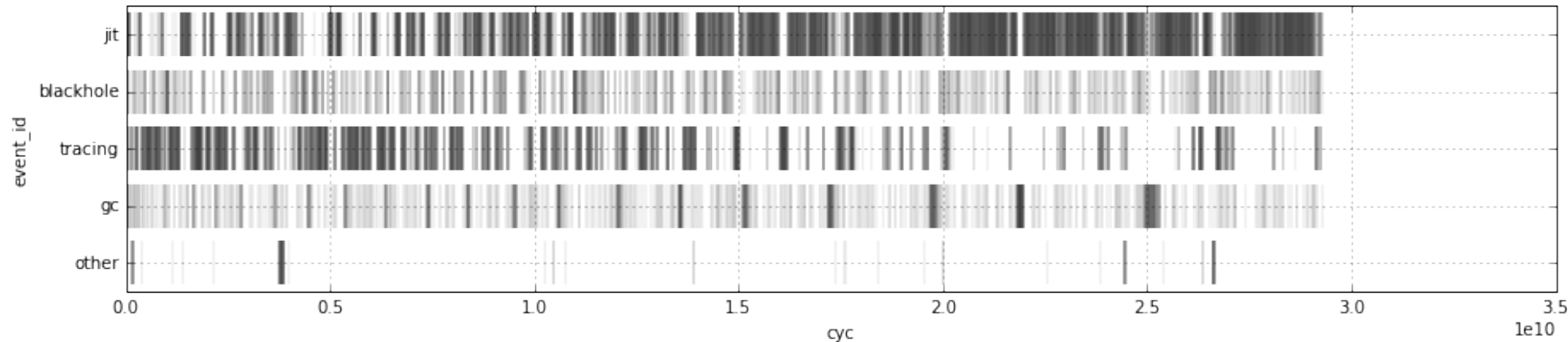
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# Pydgin in Our Research Group

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- Statistics for software-defined regions
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- Control- and memory-divergence for SIMD
- Basic Block Vector generation for SimPoint
- Analysis of JIT-enabled dynamic language interpreters



# Conclusions

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