INHERENTLY SECURE PROCESSING

Hive

The DOVER Edge

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Draper

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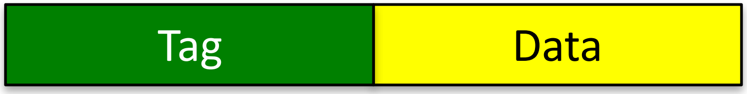
Question

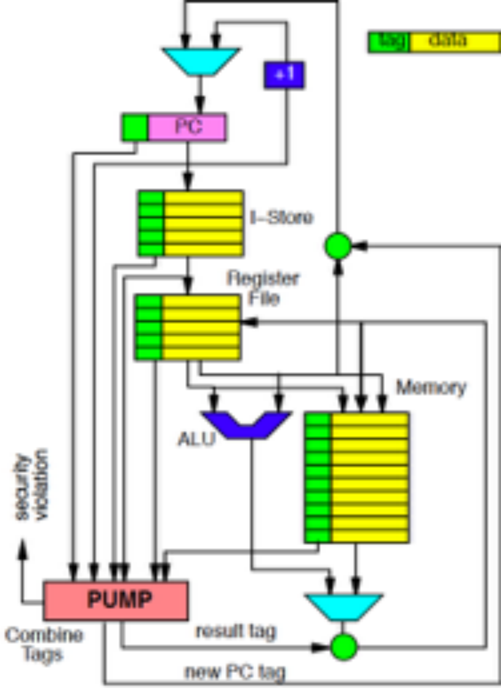
- How handle the “edge” of a tagged system, where necessary to deal with
  - I/O to the untagged world
  - Tag-oblivious, legacy devices and drivers
  - Tag-oblivious, Direct-Memory Access devices

DOVER=RISC-V + PUMP Software-Defined Metadata Processing (SDMP)



Tag

Data



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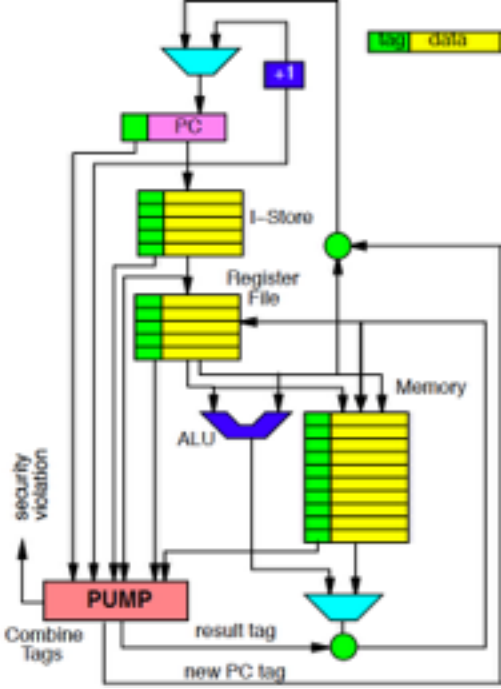

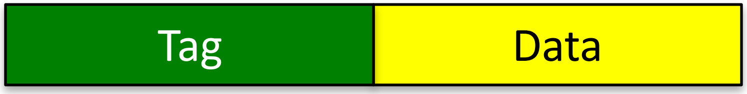

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- Add metadata tag to every word
  - Allows us to know information about data word
    - Type, where-came-from, buffer, secrecy

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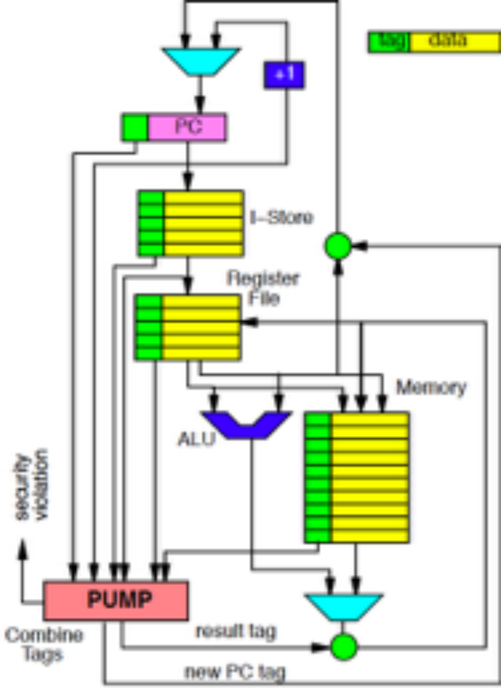

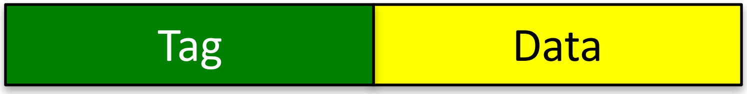

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  - Allows us to know information about data word
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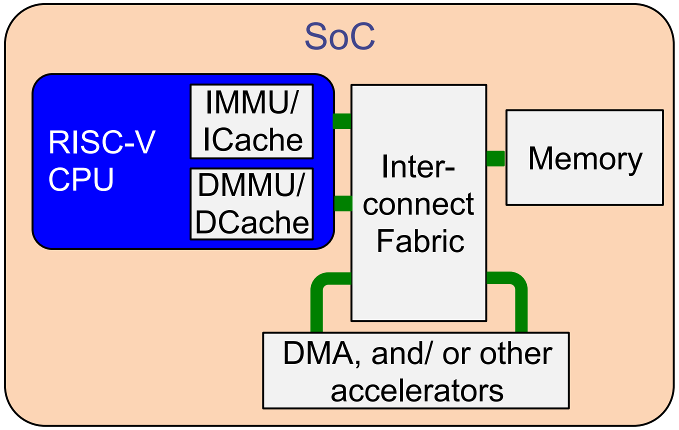
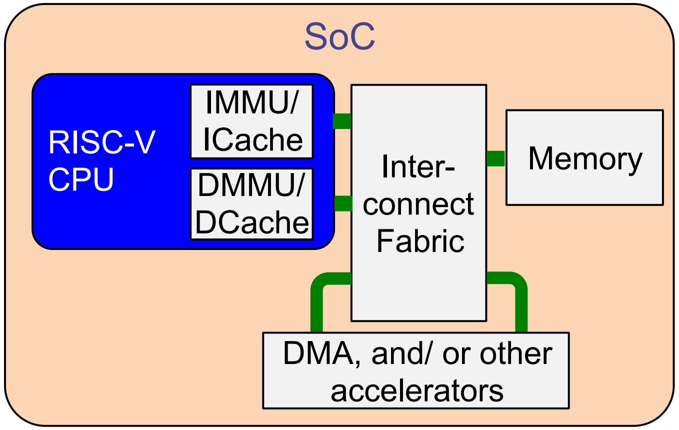
- Mediate every instruction by checking tags
  - Allows enforcement of safety/security policies
    - Memory safety, CFI, integrity, information flow

Challenge


SoC
RISC-V CPU
IMMU/ ICache
DMMU/ DCache
Inter-connect Fabric
Memory
DMA, and/ or other accelerators

Challenge

- Processor not only entity can write to memory.



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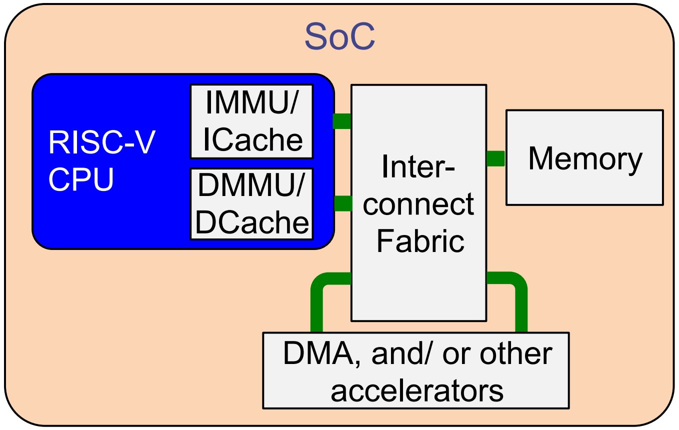

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- DMA engines for performance
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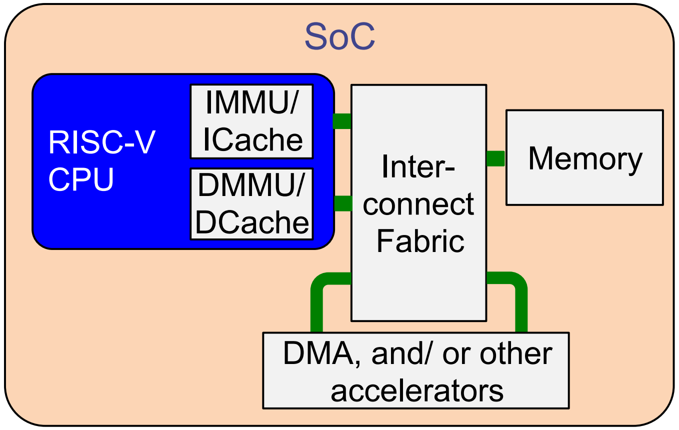
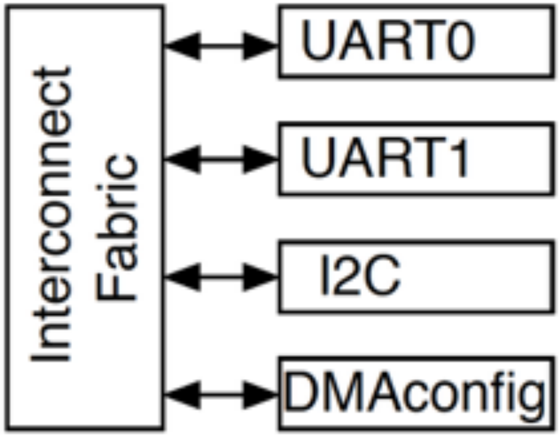
- Danger: undermine security policies
  - Write over OS code
  - Read secret data



Fine-Grained Slave Device Control



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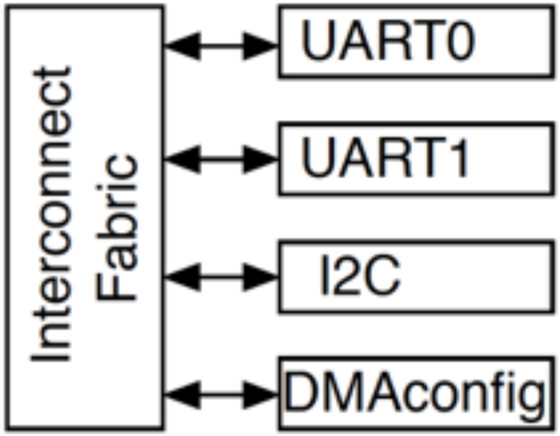

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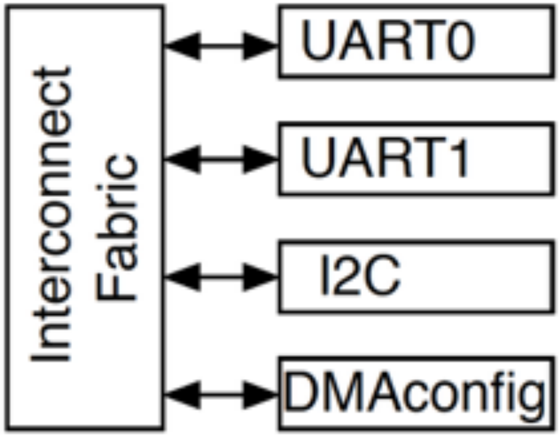

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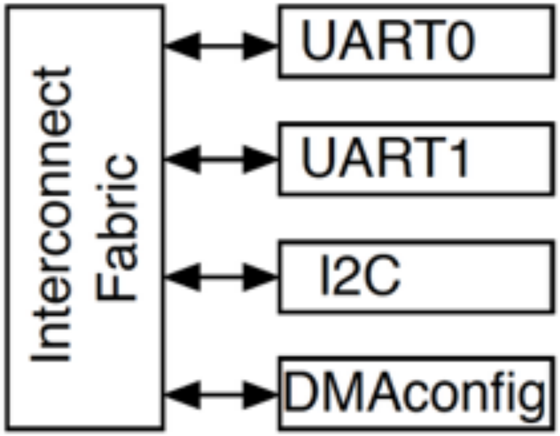

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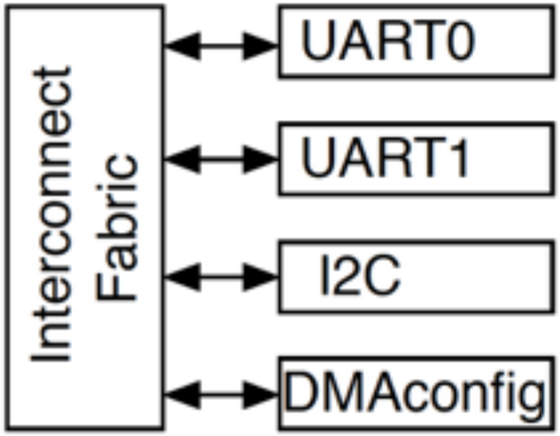
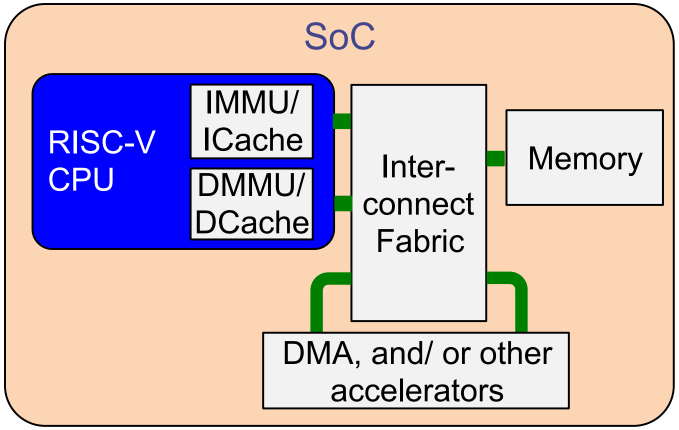
- Mark memory-mapped slave data as untrusted
  - and by source



DMA IO Policies



DMA IO Policies

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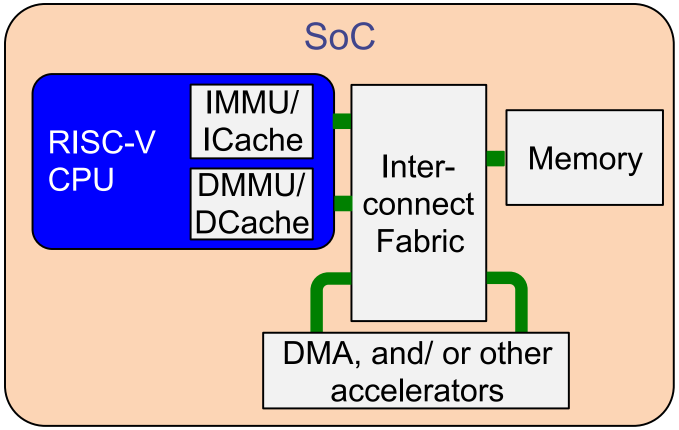

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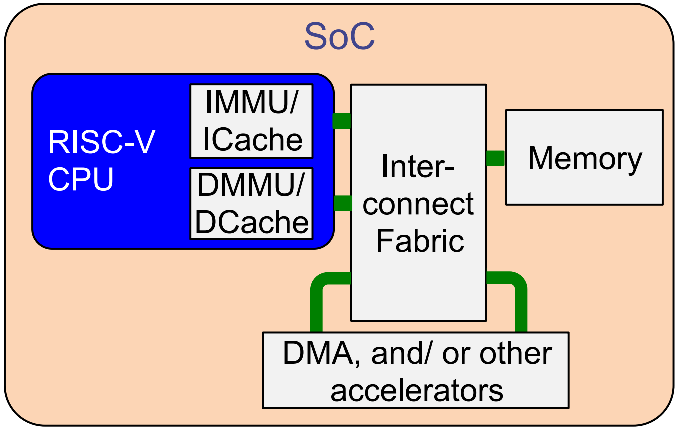

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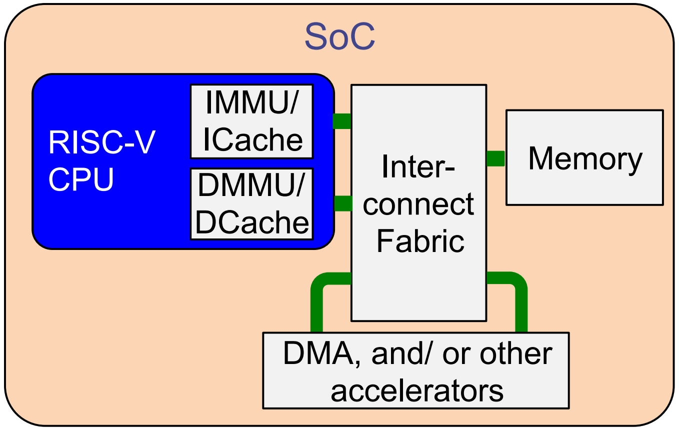

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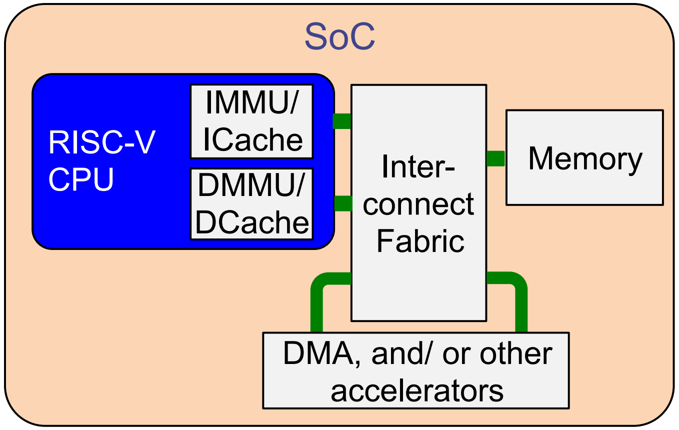
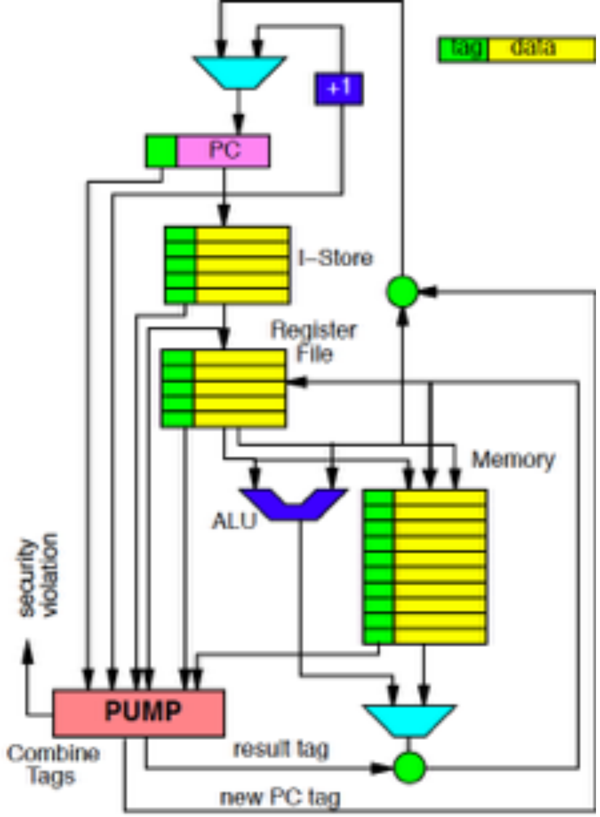
- Data presence/synchronization
  - only grab valid data
  - only overwrite empty buffer
    - and mark as non-empty when write



SDMP Policy Function



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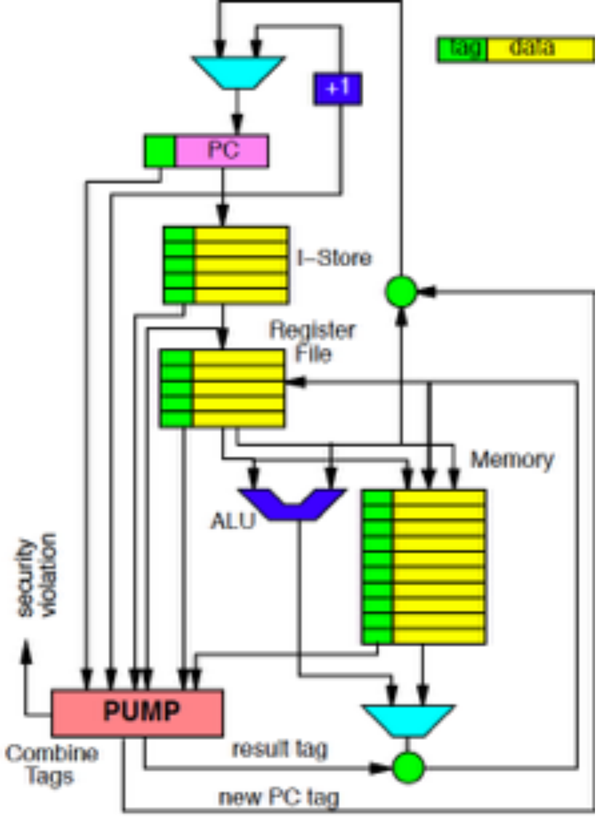

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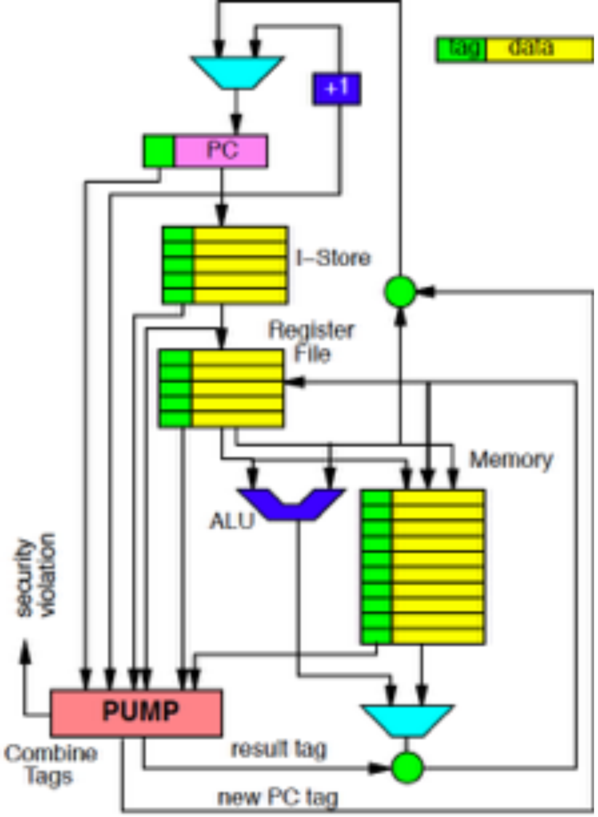

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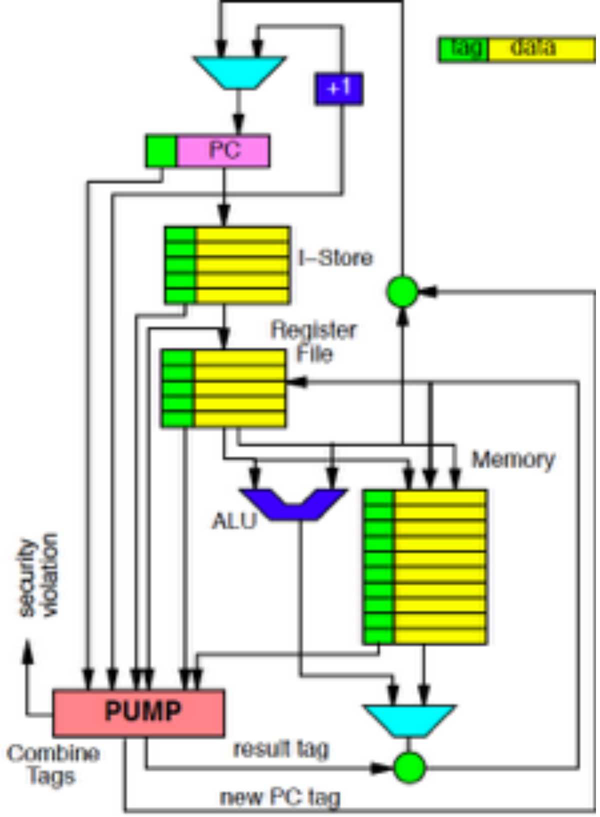

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  - PC_{tag}
  - $Result_{tag}$ (RD, memory result)

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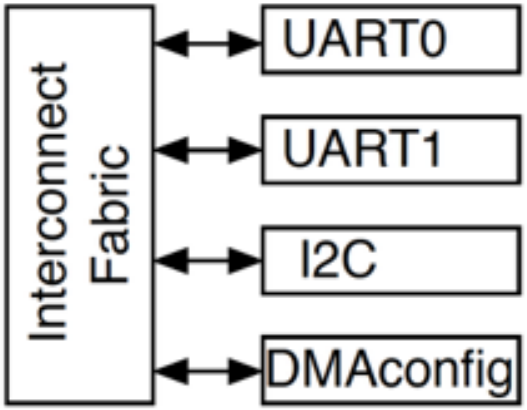

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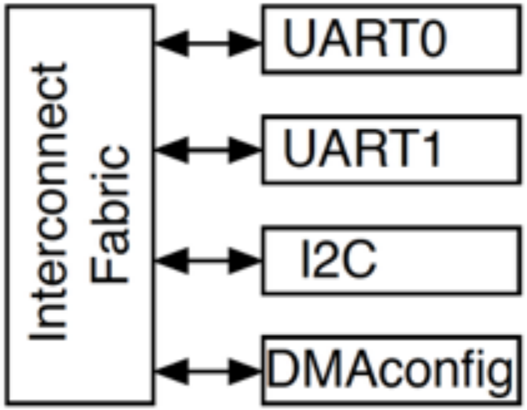

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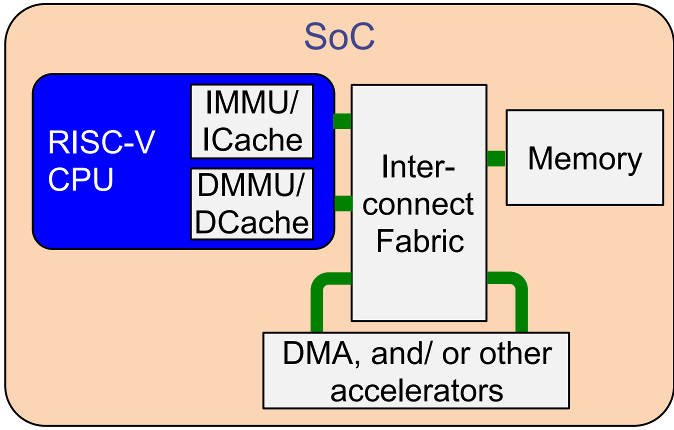

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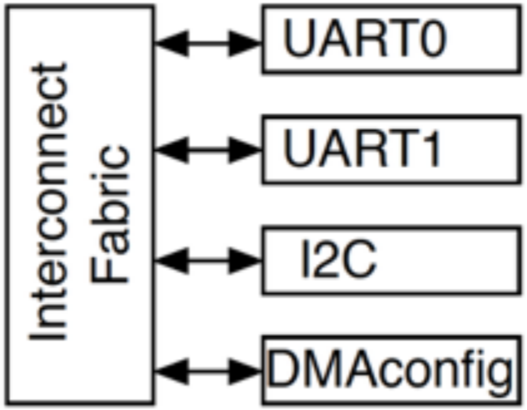

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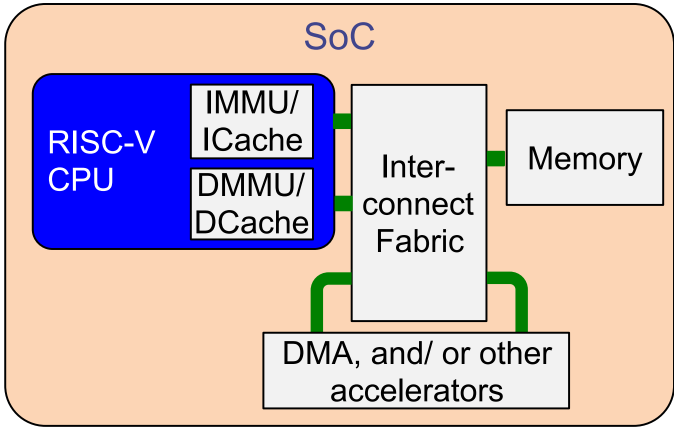

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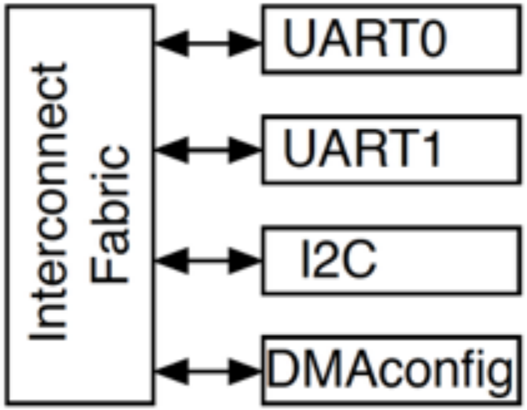

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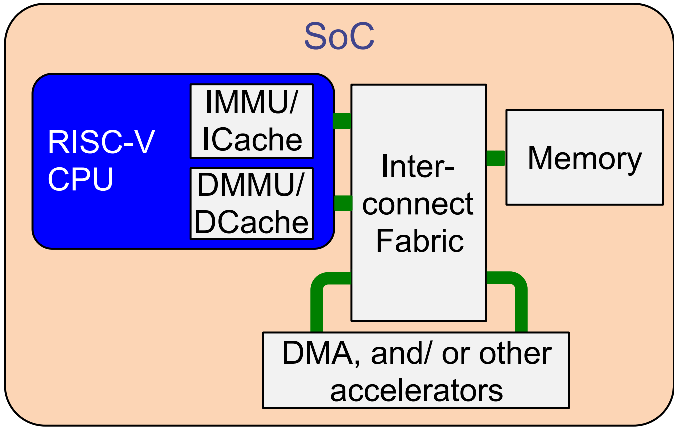

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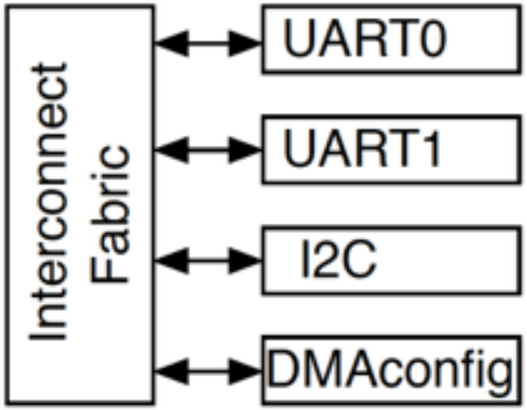

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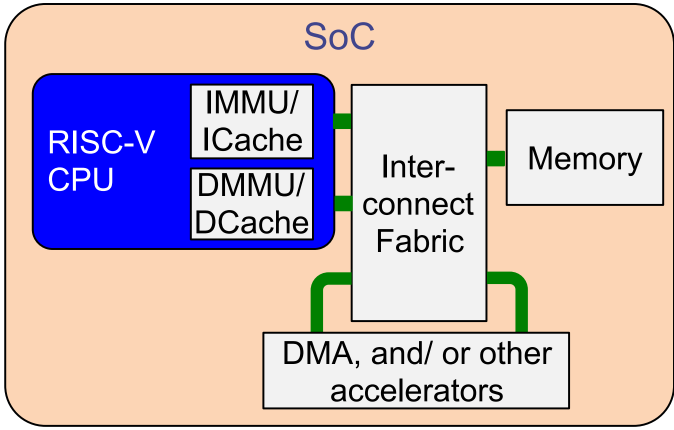

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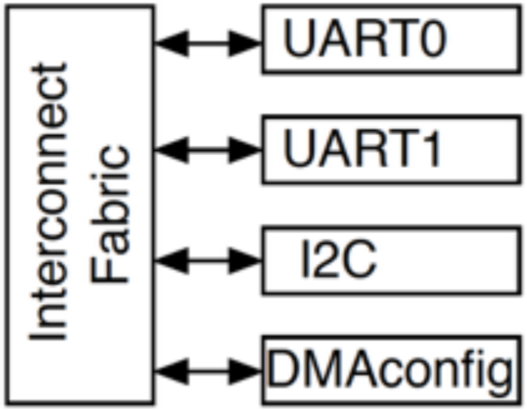

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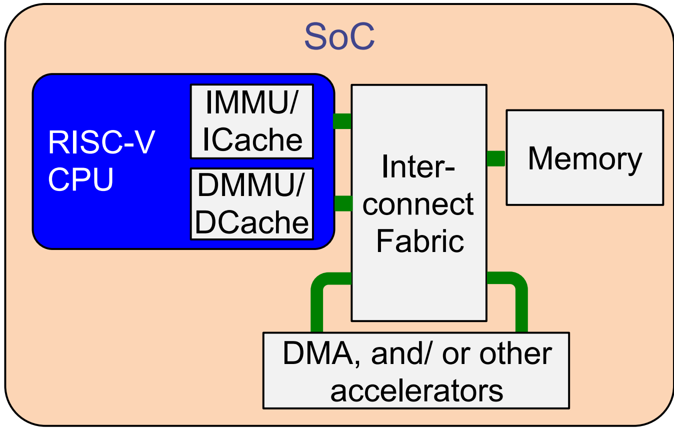

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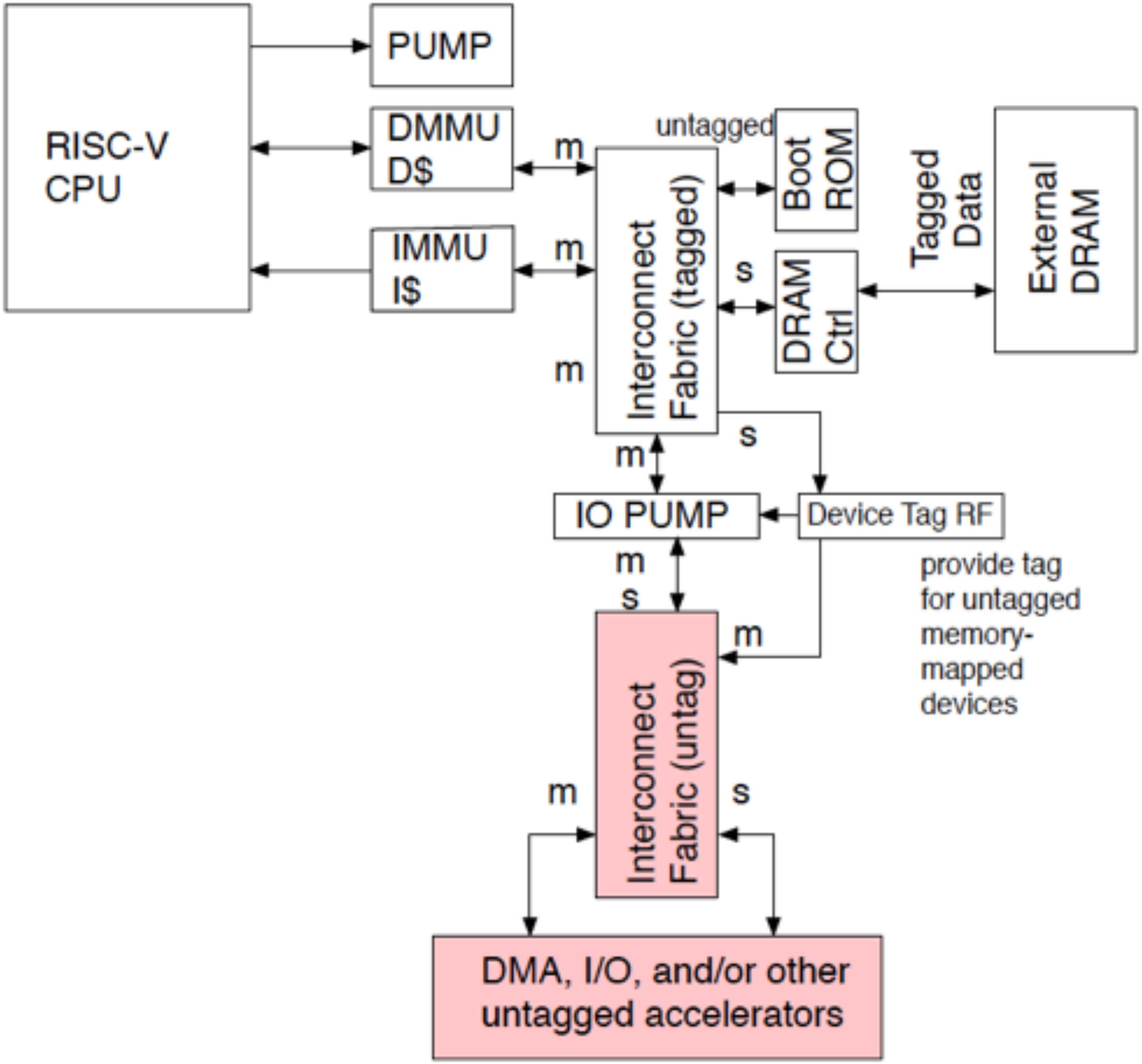
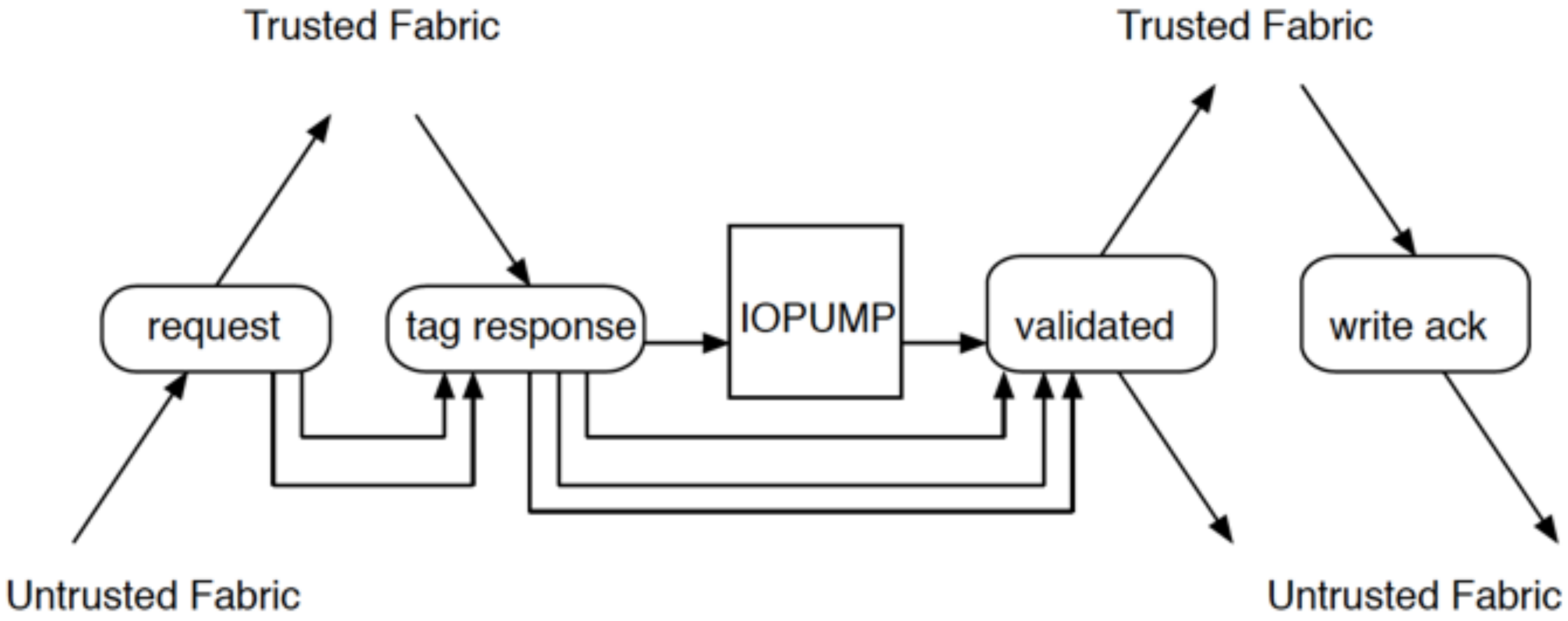
2. Discard offending operation
   - Set $Result_{tag}$ to DISCARD
     - Redact data, discard write
   - Allow device to continue

DOVER SoC Architecture



DMA Validation Architecture



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- IOPUMP CSRs similar to PUMP CSRs
  - Rule inputs and outputs

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- Insertion into
  - Memory-mapped IOPUMP CSRs
  - Instead of RISC-V PUMP CSRs

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  - For all actors, including DMA IO
- Maintain uniform SDMP model to the Edge
  - Slave device tags
  - Mediated DMA

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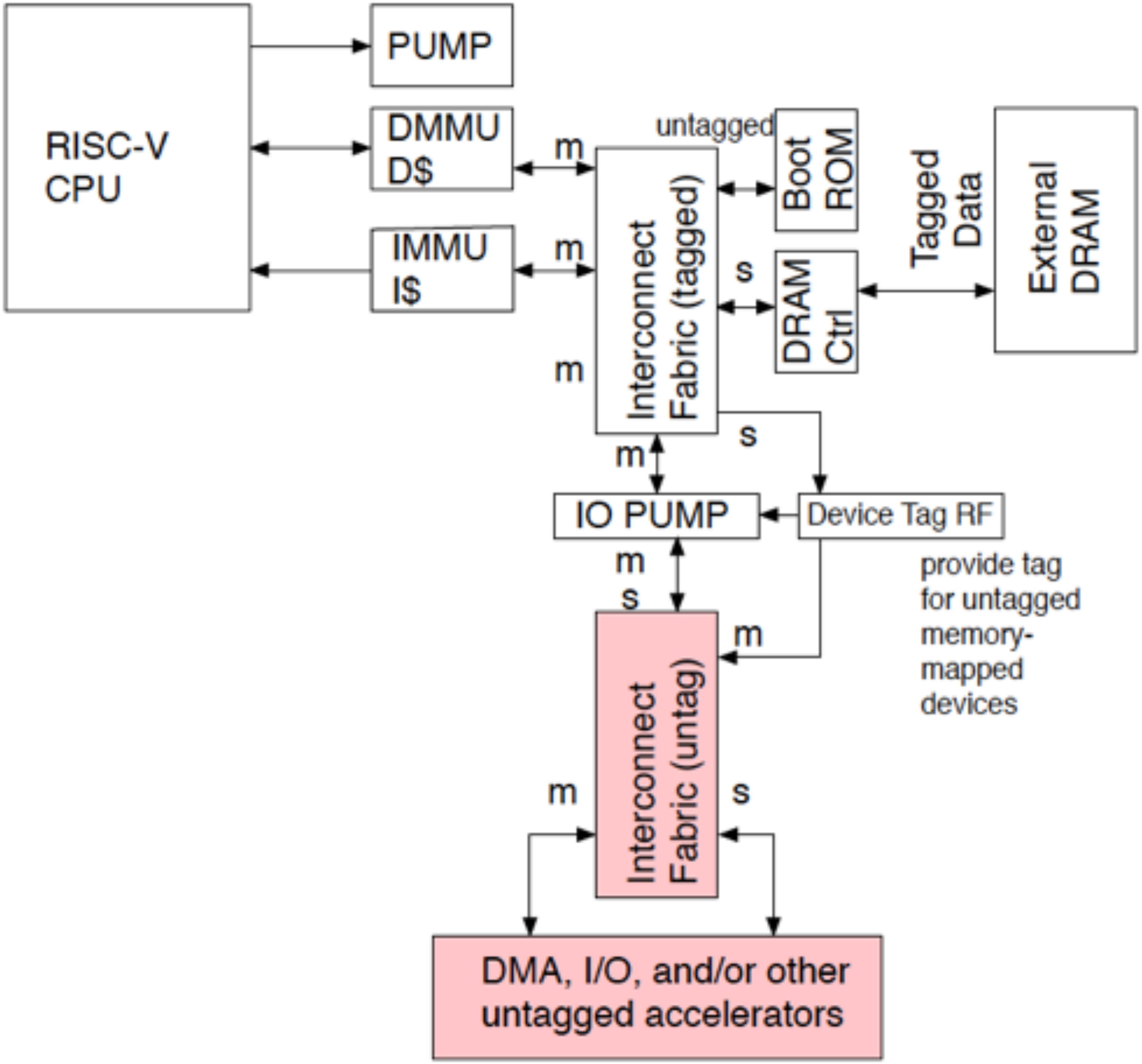

provide tag for untagged memory-mapped devices