KISS PULPino

Updates on PULPino

5th RISC-V Workshop, Mountain View (California), Florian Zaruba
Imperio

- **First** ASIC of PULPino (UMC 65)
- Complete µC (RV32IMC)
- Integrated FLL
- **Speed**: 500 MHz
- **Peripherals**:
  - 19 GPIOs, UART, I2C, SPI
  - JTAG Debug Interface
- 64 kB RAM

- **Operating Voltage**:
  - 0.9 – 1.2 V

- **Dynamic Power**:
  - 14 – 71 µW/MHz, 1.2 V
  - 3 – 15 µW/MHz, 0.9 V

- **Leakage**: 150 µW

- **Area**:
  - 700 kGE* (SoC)
  - 40 kGE* (Core)

* 1 kGE = 1.44 µm²

ETH ASIC Gallery: [http://asic.ethz.ch/](http://asic.ethz.ch/)
Parallel Ultra Low Power Platform

- L2 Memory (SRAM)
- Bus Adapter
- SPI Slave
- Debug
- I2C
- UART
- SPI Master
- GPIO

Core #1
- L0

Core #2
- L0

Core #3
- L0

Core #N
- L0

Instruction Cache (SCM)

Low Latency Interconnect

DMA

Peripheral Bus

Instruction Bus

Bus Adapter
Parallel Ultra Low Power Platform

L2 Memory (SRAM)

Bus Adapter

Core #1

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Low Latency Interconnect

DMA

Bus Adapter

Peripheral Bus

I2C

UART

SPI Master

GPIO
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Parallel Ultra Low Power Platform

- **Peripheral Bus:**
  - I2C
  - UART
  - SPI Master
  - GPIO

- **Bus Adapter**

- **L2 Memory (SRAM)**

- **Core #1**
  - L0

- **Bus**

- **Data RAM**

- **Instruction RAM**

- **SPI Slave**

- **Debug**
Current State

- RV32ICM + custom instructions
  - Hardware-loops
  - Post-incrementing load and stores
  - SIMD
- Patch for RISC-V toolchain
  - Built-ins for SIMD
  - Infers instructions
- 10x efficiency increase

- Support for all targets:
  - RTL simulation
  - FPGA mapping
  - Virtual platform
  - ASIC
  - Silicon proven core
  - 3.19 Coremark/MHz
  - 1.2 DMIPS/MHz
Multicore Cluster

- PULP
- Research
Multicore Cluster
- PULP
- Research

Standalone µC
- PULPino
- Ease of use
Multicore Cluster
- PULP
- Research

Standalone μC
- PULPino
- Ease of use

Mixed signal
- VivoSoC
- Healthcare
Open Sourcing PULPino

- We open sourced PULPino on 1st March 2016…
- … and got fantastic media coverage
- Over 15,000 users visited our website
- More than 600 unique clones on GitHub
- Over 20 companies and research institutes use PULPino
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Future of PULPino (PULPino V2)

- Continue this success
- **PULPino V2:**
  - Support for Verilator simulation
  - IP-XACT description
  - New peripherals (µDMA)
  - New, streamlined event unit
  - SDK
  - Updated compiler
  - Improved documentation and tutorials

1. **March 2016**
   - First release of PULPino

2. **May 2016**
   - Toolchain for our modified RISC-V implementation

3. **May 2016**
   - DSP oriented extensions

4. **Q1 2017**
   - PULPino V2

5. **Late 2017**
   - PULPino V3, Virtual platform (ISS)
Future Efforts
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Privileged ISA

- Secure PULPino, MMU
- Sel4 OS
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- Secure PULPino, MMU
- Sel4 OS

< 10 kGE RISC-V

- RV32 IC
- 1 & 3 stage pipeline
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< 10 kGE RISC-V
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Heterogeneous configuration
- FPU
- Accelerators
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Check us out on:

- https://github.com/pulp-platform
- https://twitter.com/pulp_platform
- http://www.pulp-platform.org
Questions?

www.pulp-platform.org

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