Technical Committee Update

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- To upstream the software development tools (compiler, debugger, etc.)
- To maintain and update a list of hardware implementations of the architecture

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- Provide guidelines for platform integration to avoid fragmentation in the RISC-V software ecosystem
- Setting up program committees for future RISC-V workshops to make it a prominent venue to present in-progress work related to RISC-V

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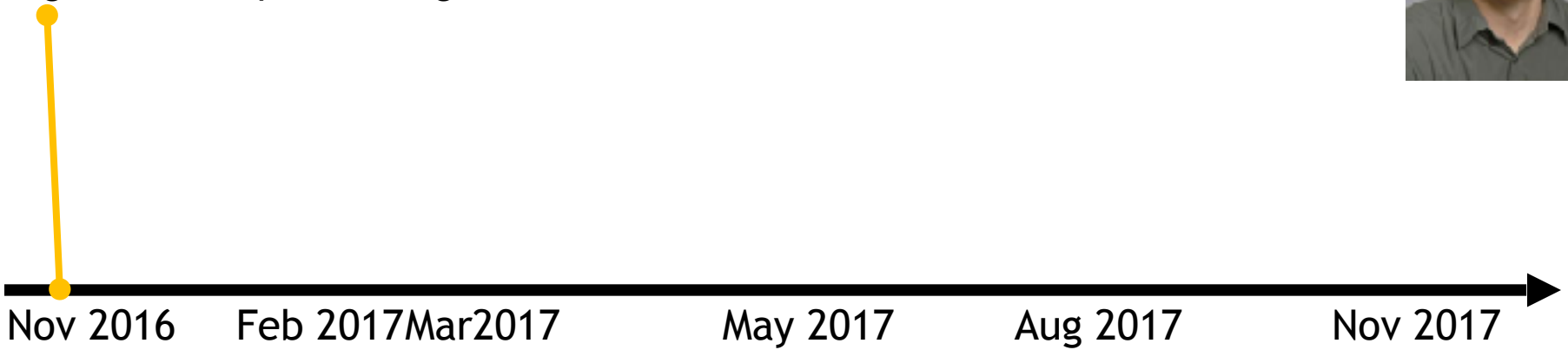
- Task groups could be added/phased out as needed

Opcode Management TG

Agree/tweak plan, assign more leaders and doers



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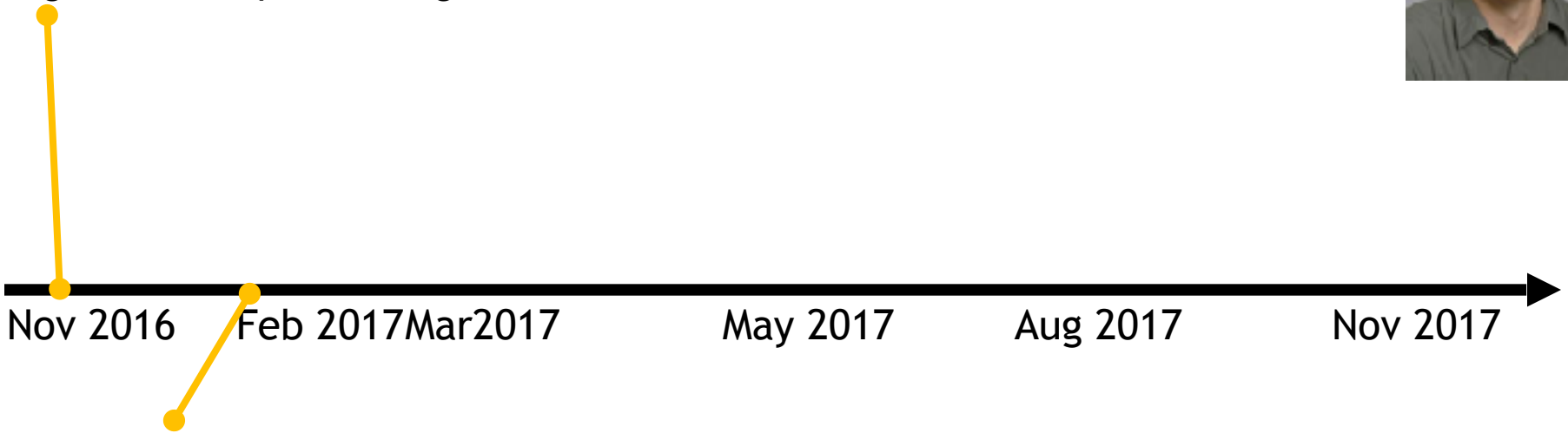

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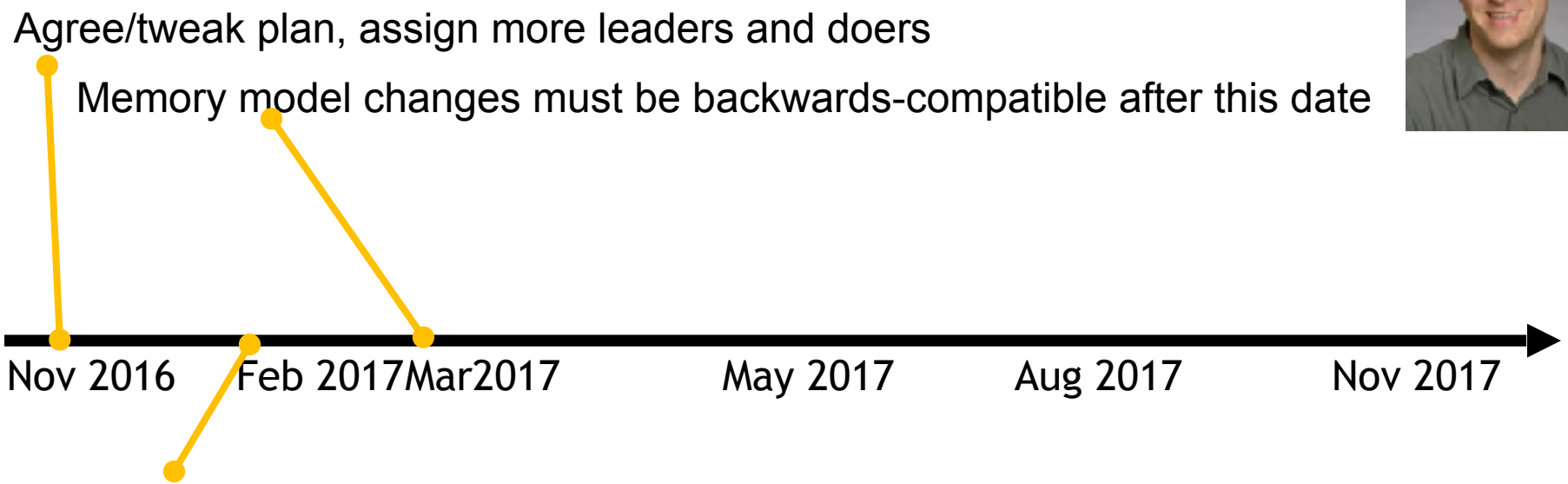

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Nov 2016 Feb 2017 Mar2017 May 2017 Aug 2017 Nov 2017

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* V ratified by Foundation
* Priv-1.13.0 -> Priv-2.0 ratified?
* Complete Linux/KVM platform spec agreed, supports other OS (FreeBSD etc.)

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- Goals
  - Version 1.10 of supervisor-mode and machine-mode architecture proposal by Feb ’17
    - no backwards-incompatible changes after this point
  - Complete Unix platform spec proposal, incl. hypervisor support, by Nov ’17
  - Ratification end of ’17/beginning of ’18

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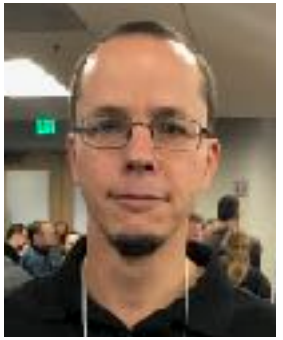
- Status
  - Basic spec: Models written in L3 (SRI), in BSV (Bluespec), in Coq (MIT)
  - Memory model: Two talks this morning

Debug Spec TG



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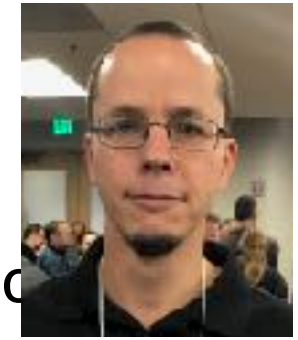

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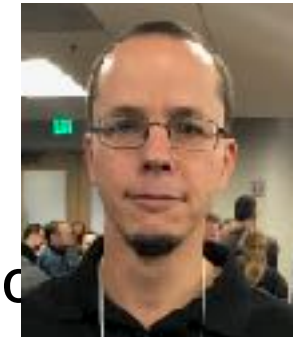

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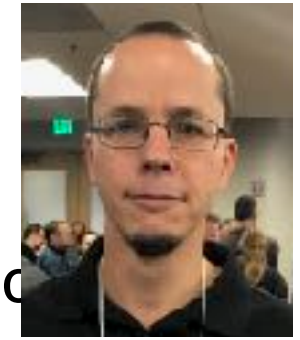

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- Goals
  - Ratification Feb ’17

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- Meetings
  - every other Wed from 6-7 PST. Meeting Thursday 1pm.

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- Goals:
  - Documenting current SW stack https://github.com/arunthomas/riscv-sw/wiki
  - Upstreaming (Binutils, GCC, LLVM, etc.)
  - QEMU: Update to priv 1.9.1, device support
  - Creating an ABI specification
  - Continue to push on Linux distribution support (e.g., Debian, Fedora)
  - Documentation
  - Docker images, cross-toolchain packages in Linux distros

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- Any questions?