

Free Chips Project:

a nonprofit for hosting open-source RISC-V implementations, tools, code

Yunsup Lee
SiFive

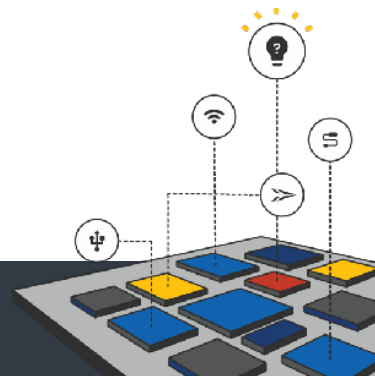
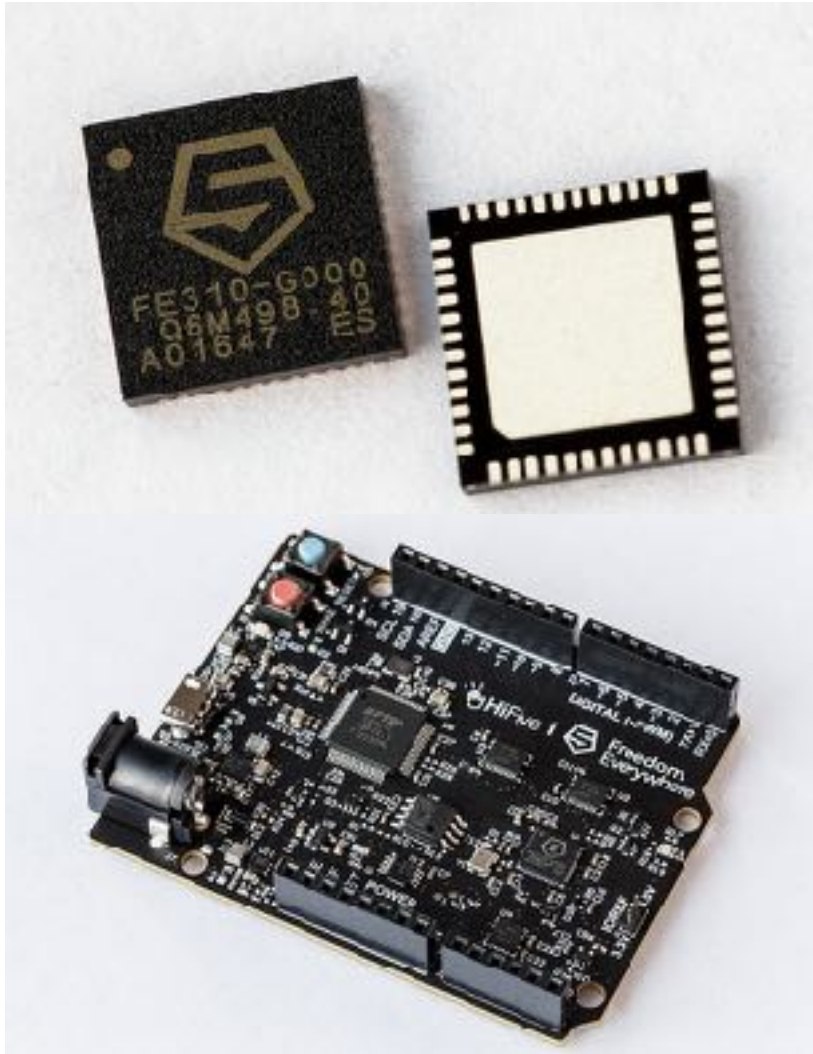


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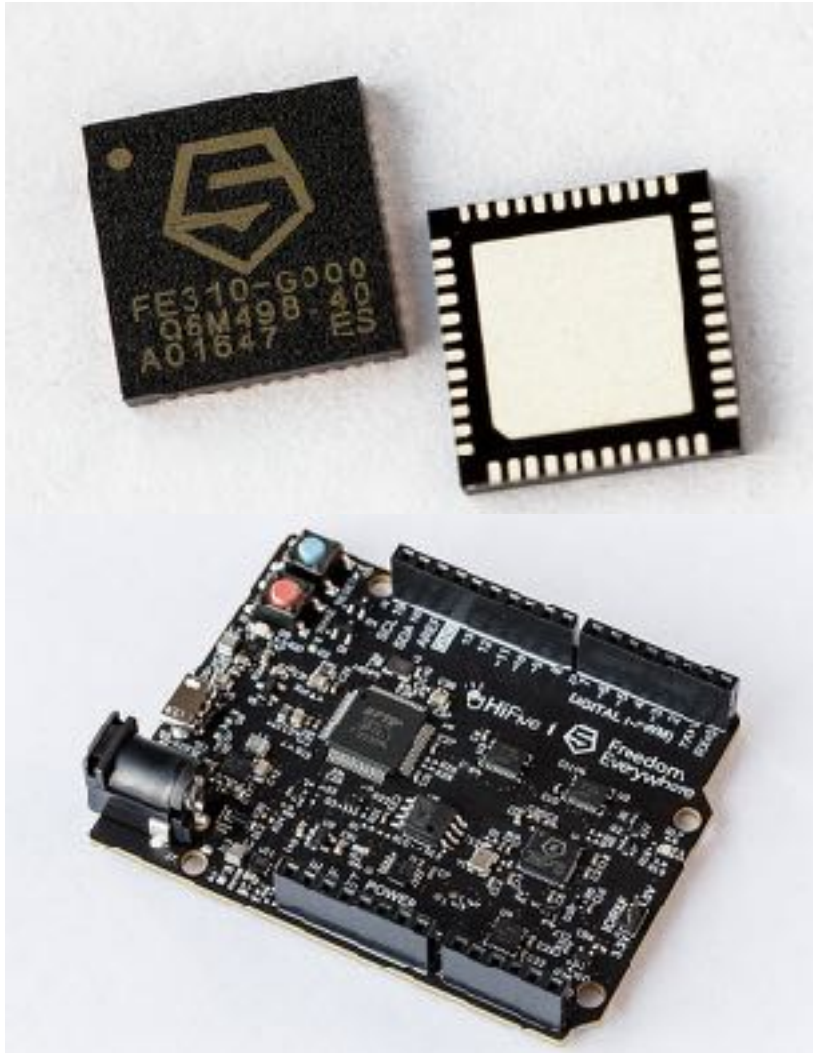


Open Source

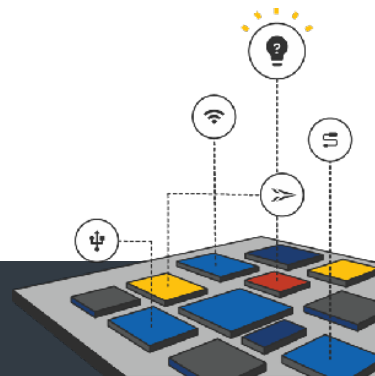
We Open-Sourced the Freedom E310 Chip!



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- RTL & FPGA scripts
 - <https://github.com/ucb-bar/rocket-chip>
 - <https://github.com/sifive/sifive-blocks>
 - <https://github.com/sifive/freedom>
- Board Support Packages (BSP)
 - <https://github.com/sifive/freedom-e-sdk>
 - <https://github.com/sifive/freedom-u-sdk>
- Documentation & Board Schematic
 - <https://dev.sifive.com>
- Forums
 - <https://forums.sifive.com>



Rocket-Chip Generator Repository Statistics

<https://github.com/ucb-bar/rocket-chip>

ucb-bar / rocket-chip

Unwatch ▾

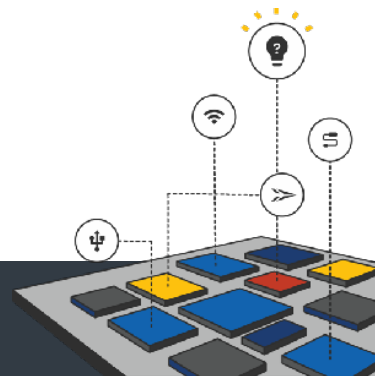
94

★ Star

187

Fork

101



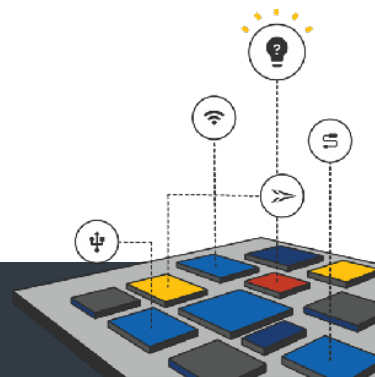

Rocket-Chip Generator Repository Statistics

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ucb-bar / rocket-chip

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3,896 commits 51 branches 0 releases 39 contributors



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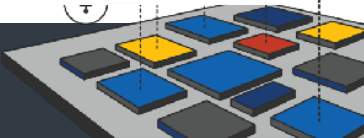
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Oct 23, 2011 – Nov 28, 2016

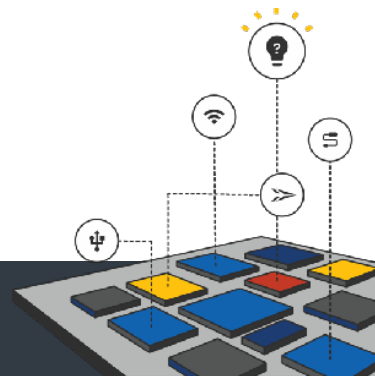
Contributions: Commits

Contributions to master, excluding merge commits



SiFive's Contribution to Rocket-Chip Repository

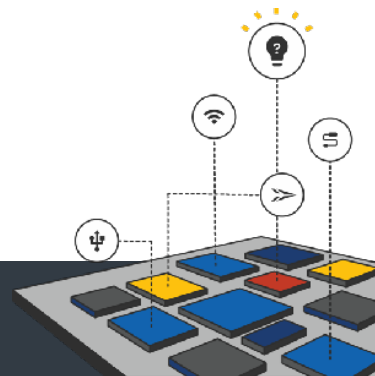
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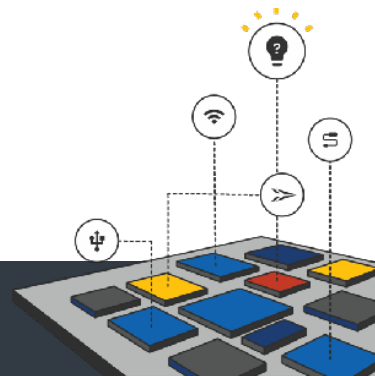
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 - Added RV32I + M/A/F support, compressed support, blocking data cache, and data SRAM options



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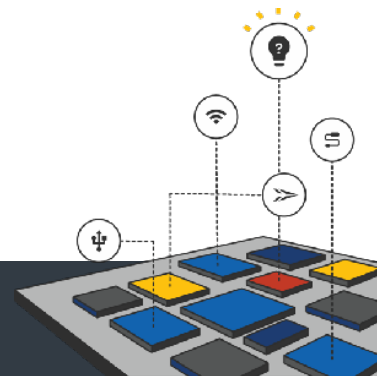
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- Diplomacy
 - Global parameter negotiation framework



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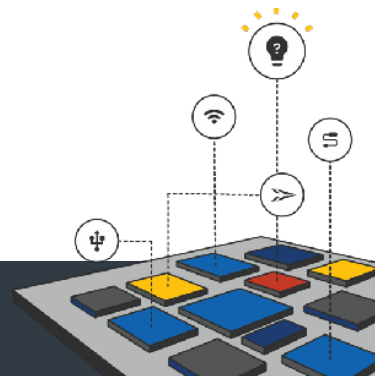
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 - Added RV32I + M/A/F support, compressed support, blocking data cache, and data SRAM options
- TileLink
 - Open cache-coherent interconnect with memory-mapped I/O support
- Diplomacy
 - Global parameter negotiation framework
- Other primitives
 - Multi-clock support, clock crossings, and asynchronous reset flops



SiFive Blocks Repository

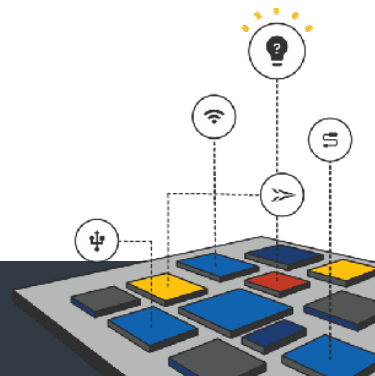
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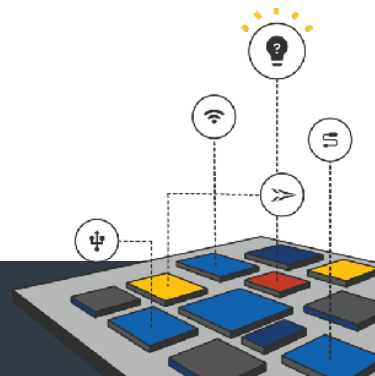
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 - SPI, UART, PWM, GPIO, PMU
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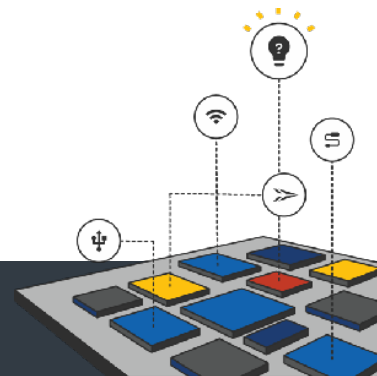
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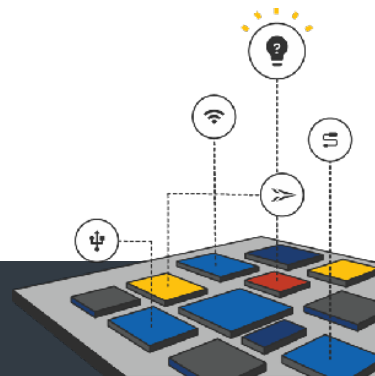
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- Low-speed Peripherals
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- High-speed Xilinx FPGA Peripherals
 - Wrappers for MIG DDR block and PCIe block
- Our vision to make a plug-and-play SoC generator starts with these reusable building blocks



Freedom Repository

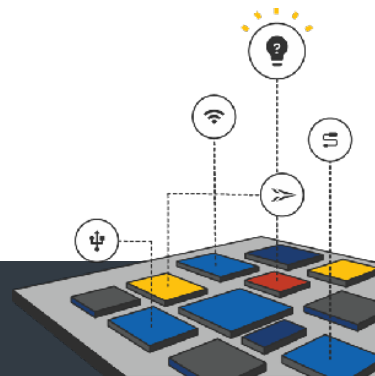
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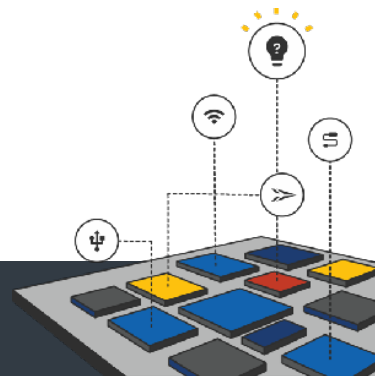
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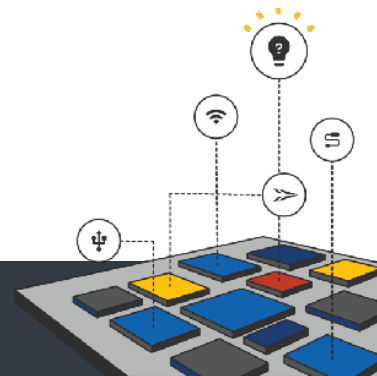
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 - Serves as a good baseline to build an SoC with your own custom blocks



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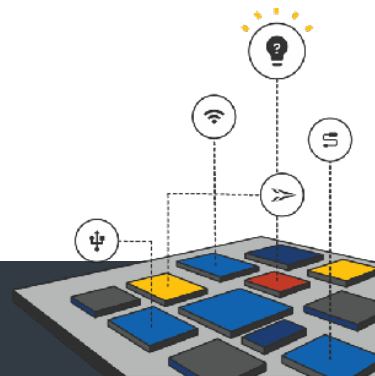
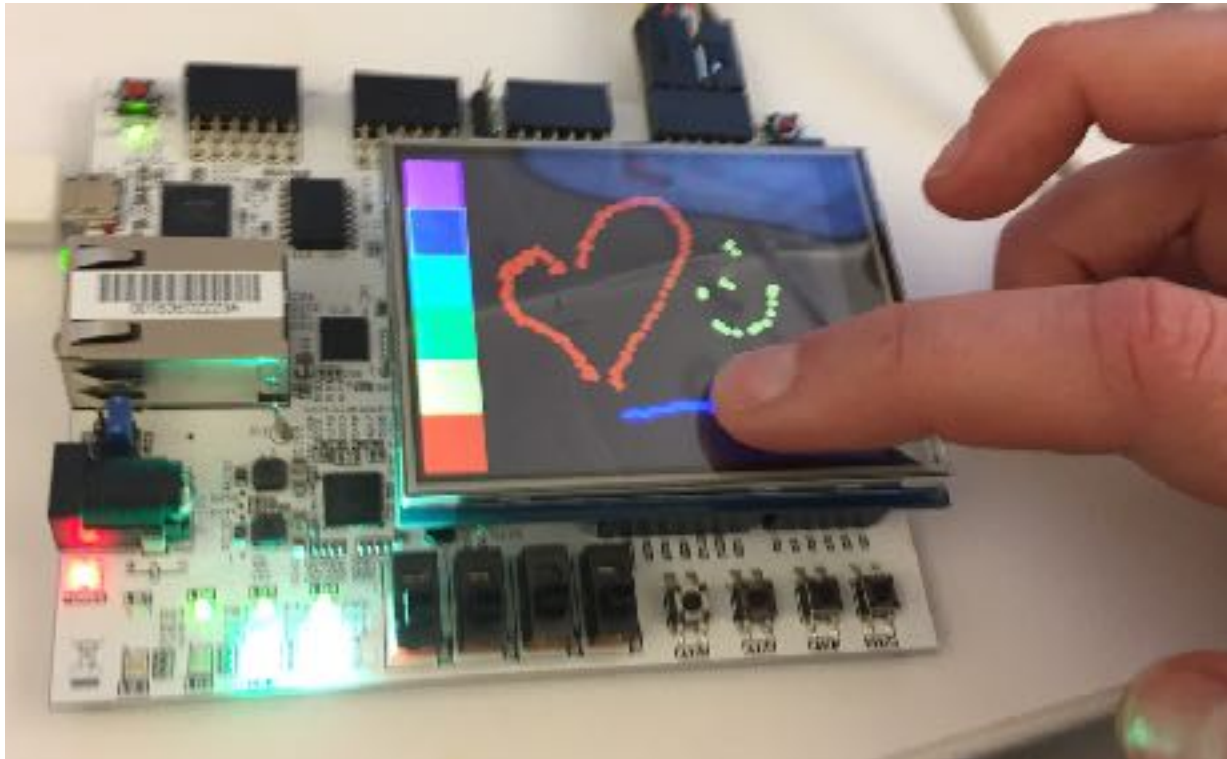
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- Submodules both rocket-chip and sifive-blocks
- Top-Level SoC Integration
 - Serves as a good baseline to build an SoC with your own custom blocks
- FPGA scripts are also open-sourced
 - Freedom E300 Arty FPGA Dev Kit
 - Freedom U500 VC707 FPGA Dev Kit



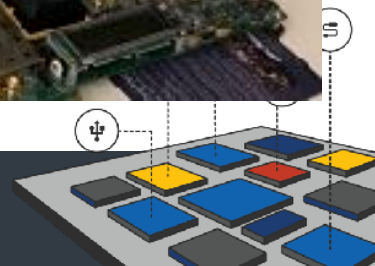
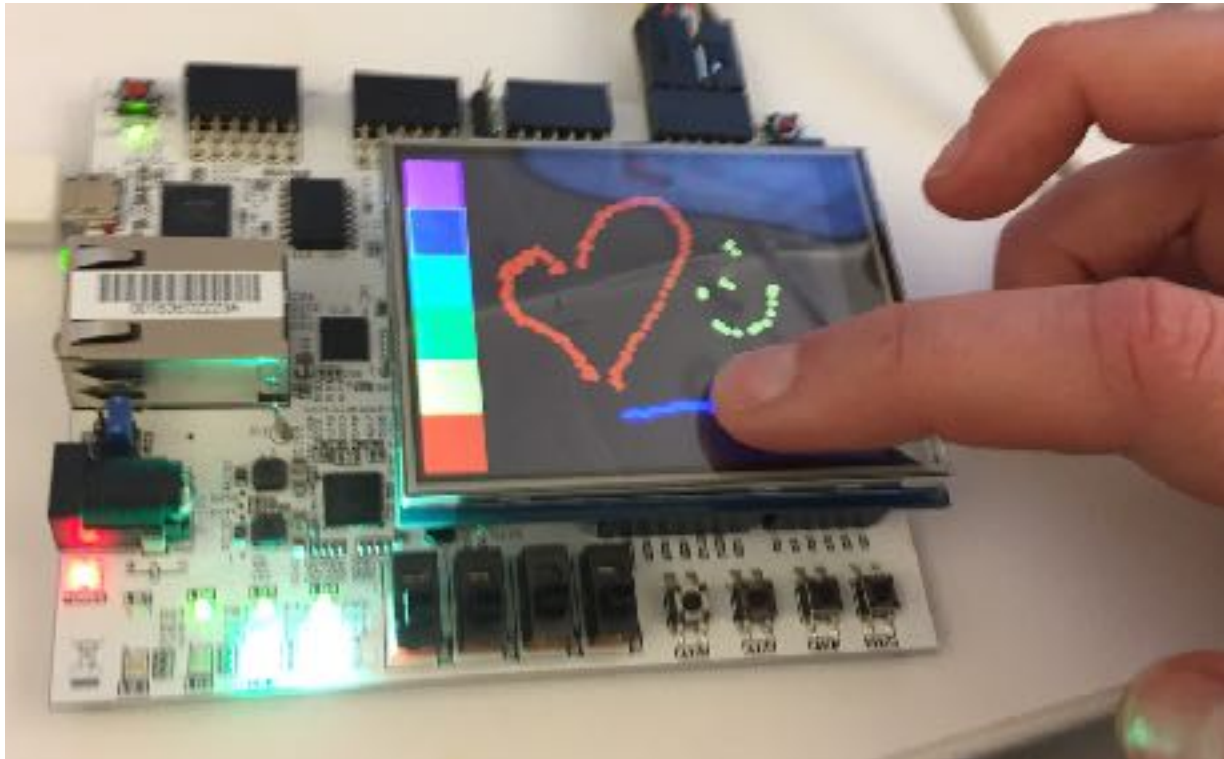
Freedom FPGA Dev Kits

Start prototyping your innovative ideas on Freedom platforms!



Freedom FPGA Dev Kits

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**But, it takes a village
to make open-source
hardware real**

Launching the “Free Chips Project”

Non-Profit “Home” for Open-Source Codebase

- Mission: Home for Open-Source Codebase to Enable Faster, Better, Cheaper Chips
- Initial contributions from SiFive and Berkeley
- Call for participation!
- Any questions?

Purpose

Sustain and evolve open-source software tools and HDL code for system-on-chip (SoC) design

Ensure free and open contributions are available to all of the SoC design community

Manage publicly accessible, online repositories of source code, documentation and issues

