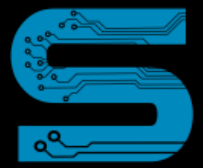

Syntacore™
Custom cores and tools

SCRx: family of the synthesizable RISC-V cores

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5th RISC-V workshop
Nov 29-30 2016

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Outline

- Introduction
- SCRx cores overview
- Summary

Syntacore introduction

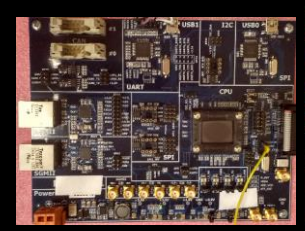
IP company

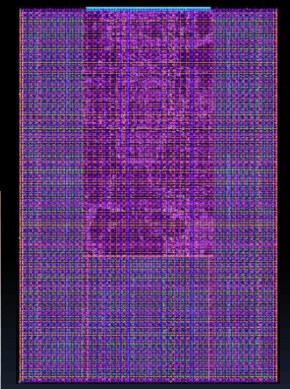
1. Develops and licenses energy-efficient programmable cores
   - with RISC-V ISA
2. Full service to specialize these for the customer needs
   - Workload analysis/characterization
   - Workload-specific customization
     - with tools/compiler support
   - IP hardening at the required library node
   - SoC integration and SW migration support

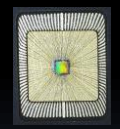
Baseline SCRx cores

SCRx: a family of the state-of-the art RISC-V compatible synthesizable processor cores

- SCR1: RV32IC[EM]
- SCR3: RV32IMC[E]
- SCR4: RV32IMCF[D]
- SCR5: RV[32|64]IMC[AFD]







Stable, configurable, available for evaluation

Baseline: every core can be extended/customized

SCR1

Minimalistic MCU core for deeply embedded applications

- RV32IC[E|M] ISA
- <20kGates in basic untethered configuration (ICE)
- 2 or 3 stages pipeline
- M-mode only
- Optional configurable IPIC
  - 8..32 IRQs
- Optional integrated Debug Controller
  - OpenOCD compatible
- Optional area-optimized MUL/DIV unit

SCR3

High-performance MCU core

- RV32IMC[E] ISA
- advanced BP, fast MUL/DIV
- Integrated IRQ controller, debug
- U- and M-mode
- optional MPU
- optional TCM/L1 caches
- up to 1.7 DMIPs/MHz, 3.16 Coremark/MHz

DEMO: freeRTOS/Coremark, running on the 28nm SCR3-based SoC

SCR4

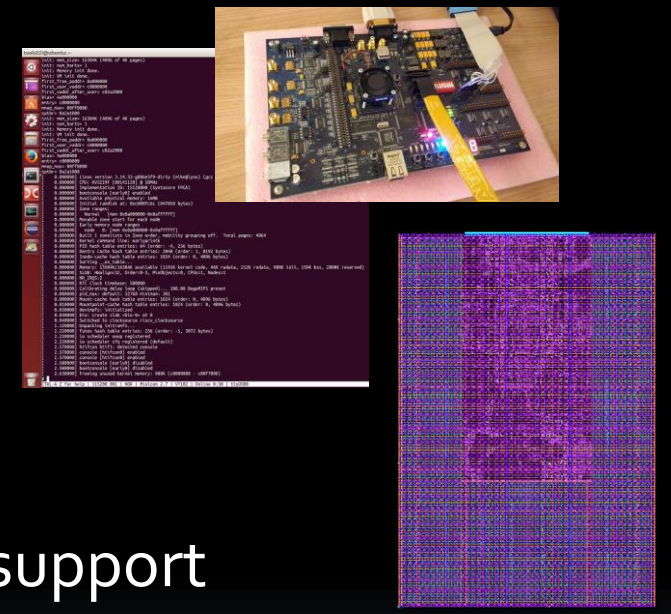
MCU core with high-performance FPU

- RV32IMCF[D] ISA
- advanced BP, fast MUL/DIV
- Integrated IRQ controller, debug
- U- and M-mode
- optional MPU, TCM
- configurable single- or double-precision FPU
  - IEEE 754-2008 compliant
  - Up to 0.7 WMIPs/MHs

SCR5

Efficient mid-range APU/embedded core

- RV32IMC[AFD] ISA, 64bit option
- Advanced BP (BTB/BHT/RAS)
- M-, S- and U-modes
- L1, L2 caches with coherency
- Full MMU, Linux, network, debug
- Single-, dual- and quad-core configurations support
- 1GHz+ @28nm
- 1.5+ DMIPs/MHz per core



DEMO: Dining philosophers @ FPGA-based Linux SDK

Near-term plans

- Privileged ISA 2.0
- Trace support
- Adding more cores to the family

Summary

- Introducing family of RISC-V cores:
  - Stable, clean-slate baseline designs
  - Highly-configurable and customizable
  - Available for evaluation
  - Support
- Demos at the poster session

Thank you!