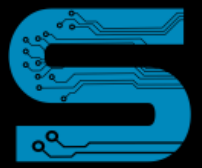

Syntacore™
Custom cores and tools

SCRx cores family demos

Pavel Khabarov

6th RISC-V workshop
May 8-11 2017

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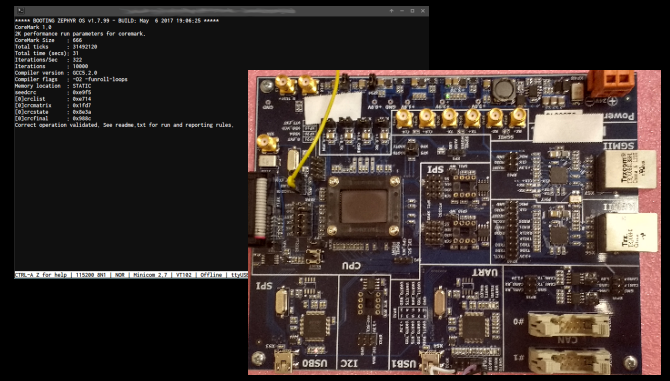
www.syntacore.com

Demo: Zephyr OS @ RISC-V-based 28nm SoC

SCR3-based 28nm SoC for industrial automation

SCR3: high-performance MCU core

- RV32IMC[E] ISA
- U- and M-mode, TCM, MPU, advanced debug



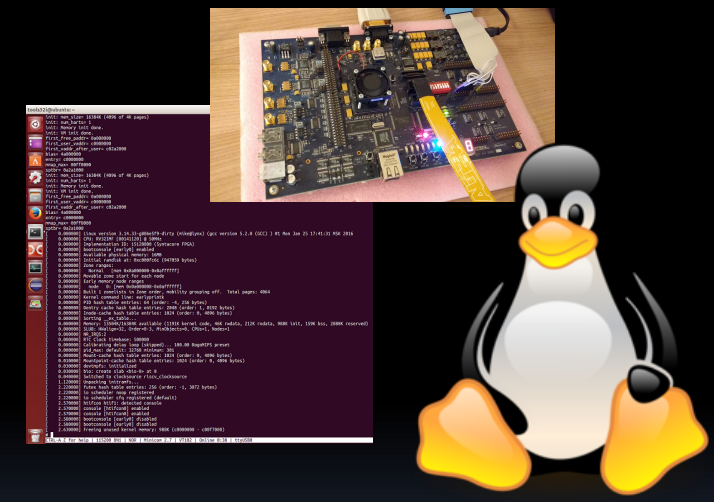
Zephyr™

The Zephyr™ Project is a scalable real-time operating system (RTOS) supporting multiple hardware architectures, optimized for resource constrained devices, and built with security in mind
https://www.zephyrproject.org/

Demo: SMP Linux @ multicore SCR5-based System

SCR5-based dual-core SMP Linux SDK running

Dining philosophers multithreaded benchmark



SCR5: Efficient mid-range APU/embedded core

- RV32IMCAFD ISA
- Dual- and Quad-cores configs support
- Full MMU, M-, S-, U-modes
- L1, L2 caches with coherency
- 1GHz+ @28nm

Demo: SCR5 Extensibility Example

Demo: Custom extension set for AES acceleration used by OpenSSL in Linux env

- More than 54x speedup
- Data
  - RV32G – FPGA-based devkit, riscv gcc, optimized C++ implementation
  - Rv32G + custom extension

case	clock, MHz	score, MB/s	score, MB/s per GHz	speed-up
RV32g	20	0.222	11.1	^
RV32g + custom	20	12.040	602	54.2

Disclaimer: Authors are aware AES allows for more efficient dedicated accelerators designs, used as example algorithm

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Custom cores and tools

Demo: other application examples

Thank you!