Demo System Architecture
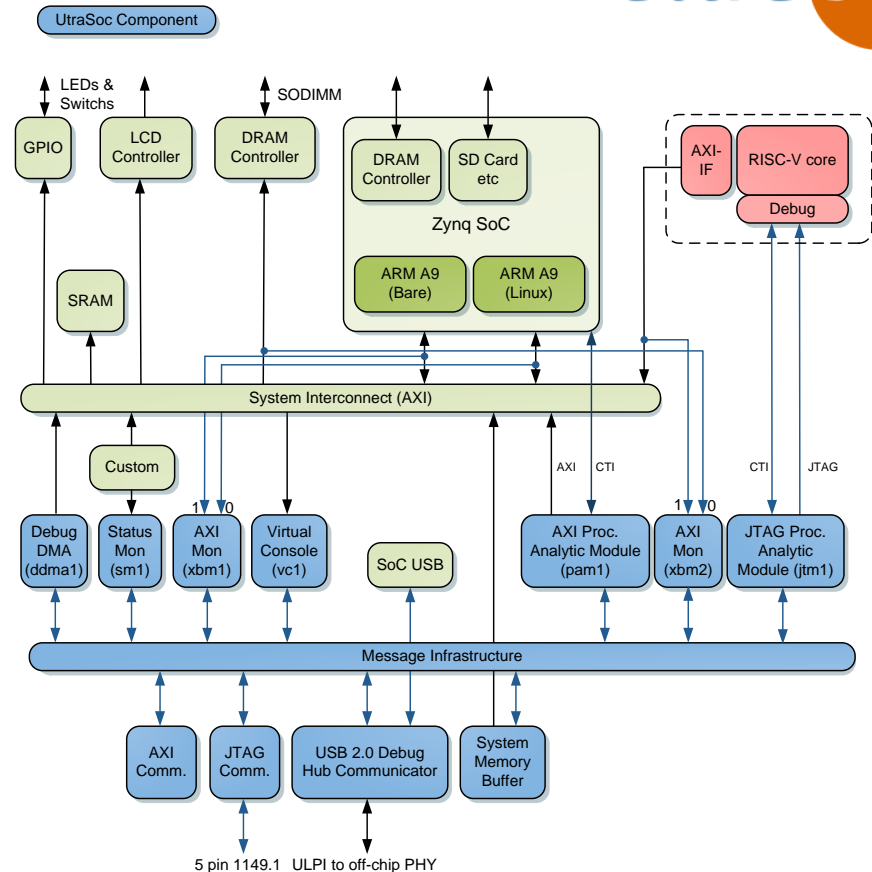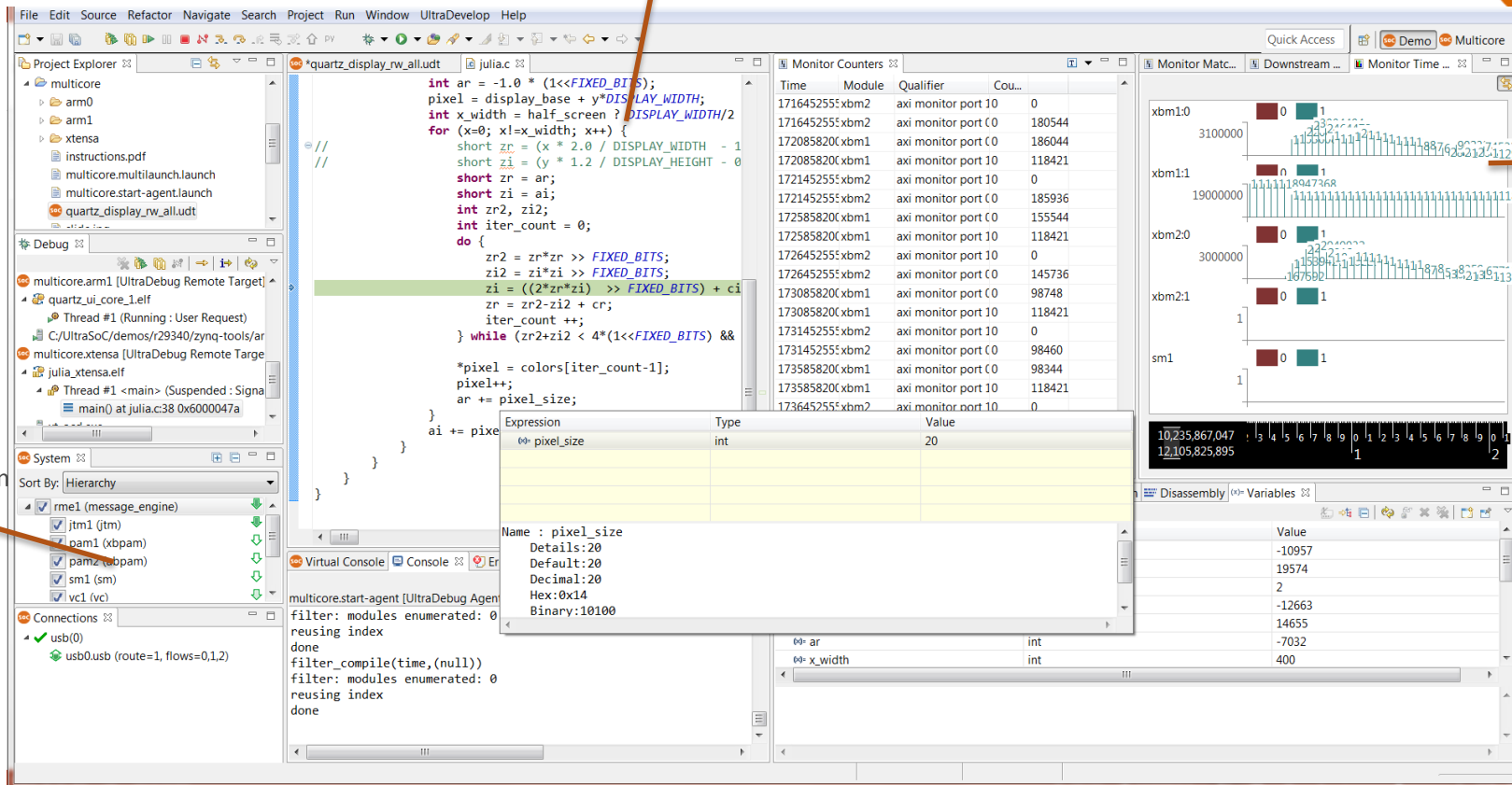
- Zynq FPGA platform
  - ARM
  - Rocket RV32 RISCV
  - custom logic
- Demo shows:
  - Bus state
  - Traffic
  - Performance histogram
  - Memory
  - Processor control

UltraSoc Component

LEDs & Switchs

SODIMM

GPIO | LCD Controller | DRAM Controller

DRAM Controller | SD Card etc

Zynq SoC

ARM A9 (Bare) | ARM A9 (Linux)

AXI-IF | RISC-V core

Debug

SRAM

System Interconnect (AXI)

Custom

AXI CTI | CTI JTAG

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Debug DMA (ddma1) | Status Mon (sm1) | AXI Mon (xbm1) | Virtual Console (vc1) | SoC USB | AXI Proc. Analytic Module (pam1) | AXI Mon (xbm2) | JTAG Proc. Analytic Module (jtm1)

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Message Infrastructure

AXI Comm. | JTAG Comm. | USB 2.0 Debug Hub Communicator | System Memory Buffer

5 pin 1149.1   ULPI to off-chip PHY

Demonstration Features

- **Heterogeneous multi-core + Custom logic**

- 2 x ARM A9 + Rocket RISC-V

- Processor status & code visibility (three processors)

- AXI Bus Monitor counters (read/write bytes) & trace

- Status Monitor for custom logic (FIFO, traffic source + sink)

- UltraSoC DMA access (read/write to system memory)

- Heterogeneous CPU run and halt

- USB 2.0 Debug Hub connectivity

- Deadlock detection

UltraSoC IDE

Visibility of software

Bus activity

Control configuration