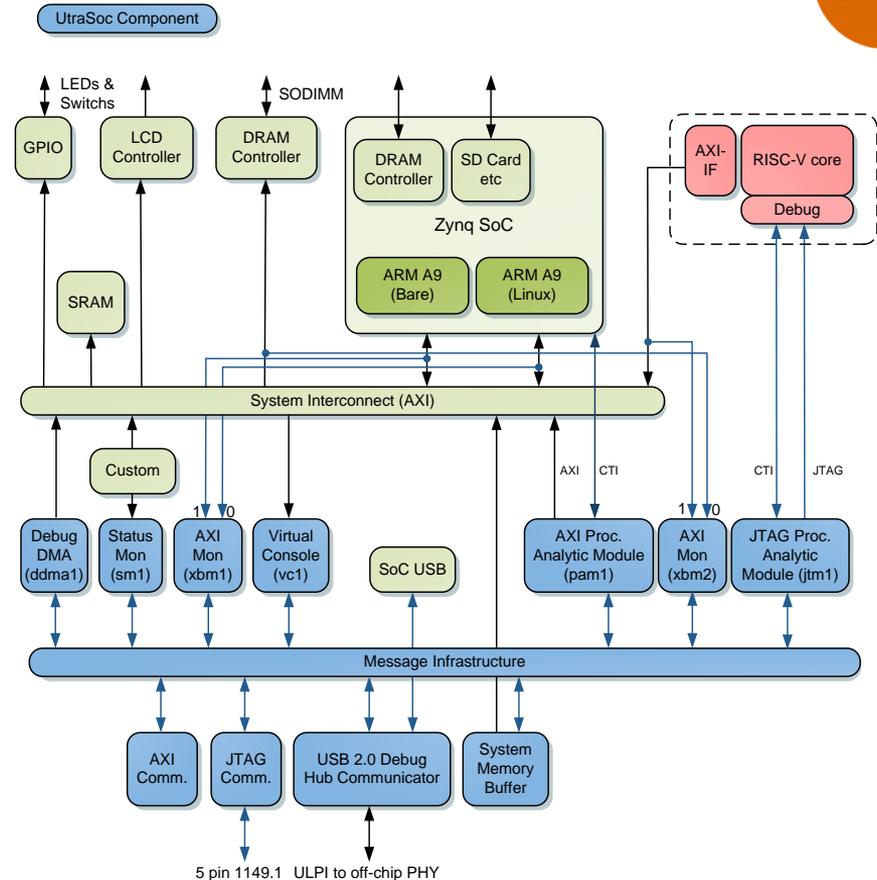


# Demo System Architecture

- Zynq FPGA platform
  - ARM
  - Rocket RV32 RISC-V
  - custom logic
- Demo shows:
  - Bus state
  - Traffic
  - Performance histogram
  - Memory
  - Processor control



## Demonstration Features

- **Heterogeneous multi-core + Custom logic**
- 2 x ARM A9 + Rocket RISC-V
- Processor status & code visibility (three processors)
- AXI Bus Monitor counters (read/write bytes) & trace
- Status Monitor for custom logic (FIFO, traffic source + sink)
- UltraSoC DMA access (read/write to system memory)
- Heterogeneous CPU run and halt
- USB 2.0 Debug Hub connectivity
- Deadlock detection

Visibility of software

Control configuration

Bus activity

The screenshot displays the UltraSoC IDE interface with several key components:

- Project Explorer:** Shows a project structure with folders for 'multicore', 'arm0', 'arm1', and 'xtensa', along with various launch and configuration files.
- Debug Console:** Lists debug targets including 'multicore.arm1', 'quartz\_ui\_core\_1\_elf', and 'multicore.xtensa'. It shows a suspended thread at 'main()' in 'julia.c'.
- System Hierarchy:** A tree view showing components like 'rme1 (message\_engine)', 'itm1 (itm)', 'pam1 (xbpam)', 'pam2 (xbpam)', 'sm1 (sm)', and 'vc1 (vc)'. It also shows 'usb(0)' and 'usb0.usb' connections.
- Code Editor:** Displays C code for a display routine. A variable 'pixel\_size' is highlighted, and a tooltip shows its details: Name: pixel\_size, Details: 20, Default: 20, Decimal: 20, Hex: 0x14, Binary: 10100.
- Monitor Counters:** A table showing hardware counter data for various modules and ports.
- Monitor Counter Table:**

Time	Module	Qualifier	Cou...
1716452555	xbm2	axi monitor port 10	0
1716452555	xbm2	axi monitor port 0	180544
1720858200	xbm1	axi monitor port 0	186044
1720858200	xbm1	axi monitor port 10	118421
1721452555	xbm2	axi monitor port 10	0
1721452555	xbm2	axi monitor port 0	185936
1725858200	xbm1	axi monitor port 0	155544
1725858200	xbm1	axi monitor port 10	118421
1726452555	xbm2	axi monitor port 10	0
1726452555	xbm2	axi monitor port 0	145736
1730858200	xbm1	axi monitor port 0	98748
1730858200	xbm1	axi monitor port 10	118421
1731452555	xbm2	axi monitor port 10	0
1731452555	xbm2	axi monitor port 0	98460
1735858200	xbm1	axi monitor port 0	98344
1735858200	xbm1	axi monitor port 10	118421
1736452555	xbm2	axi monitor port 10	0
- Monitor Counter Graphs:** Shows bus activity for xbm1:0, xbm1:1, xbm2:0, xbm2:1, and sm1. The graphs plot signal levels over time, with a 'Bus activity' label pointing to the xbm1:1 graph.
- Disassembly/Variables:** A window showing memory addresses and values, such as 10,235,867,047 and 12,105,825,895.