Foundation Update

6th RISC-V Workshop

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Outline

- RISC-V Background
- RISC-V Foundation Overview
- Foundation Structure
  - Membership Update
- Summary
In 2010, after many years and many projects using MIPS, SPARC, and x86 as basis of research, it was time for the Computer Science team at UC Berkeley to look at what ISAs to use for their next set of projects.

- Obvious choices: x86 and ARM
  - x86 impossible – too complex, IP issues
  - ARM mostly impossible – complex, IP issues

- So UC Berkeley started “3-month project” during the summer of 2010 to develop their own clean-slate ISA
RISC-V Background (cont’d)

- Four years later, in May of 2014, UC Berkeley released frozen base user spec
  - many tapeouts and several research publications along the way
- The name RISC-V (pronounced risk-five), was chosen to represent the fifth major RISC ISA design effort at UC Berkeley
  - RISC-I, RISC-II, SOAR, and SPUR were the first four with the original RISC-I publications dating back to 1981
- In August 2015, articles of incorporation were filed to create a non-profit RISC-V Foundation to govern the ISA
The RISC-V Foundation is a non-profit consortium chartered to standardize, protect, and promote the free and open RISC-V instruction set architecture together with its hardware and software ecosystem for use in all computing devices.
RISC-V is NOT an Open-Source Processor

- RISC-V is an ISA specification – NOT an open-source processor core
- Most of the cost of chip design is in software, so we want to make sure software can be reused across many chip designs
- The Foundation will encourage both open-source and proprietary implementations of the RISC-V ISA specification
Foundation Principles

- The RISC-V ISA and related standards shall remain open and license-free to all parties. The standard specifications shall always be publicly available as an online download.

- The compatibility test suites shall always be publicly available as a source code download.

- To protect the standard, only members (with commercial RISC-V products) of the Foundation in good standing can use “RISC-V” and associated trademarks, and only for devices that pass the tests in the open-source compatibility suites maintained by the Foundation.
Foundation Function

- official source of information about RISC-V, maintains an online repository of RISC-V documents, and promotes adoption of RISC-V by organizing both online and live events
- responsible for sustaining, evolving and open-source licensing of the RISC-V instruction set architecture and surrounding hardware and software ecosystem over time in response to changes in technology and the needs and requests of the user community
- manages licensing of the RISC-V trademarks and provides a vehicle to decide whether a project or product can use the RISC-V trademark
- maintains a directory of public-domain instruction set architecture and micro-architectural techniques, culled from publications and expired patents
- produces and sells RISC-V promotional material, the proceeds from which are used to further the goals of the Foundation
The Board of Directors consists of seven+ members, whose replacements are elected by the membership. The Board is ultimately responsible for fulfilling the Mission Statement. The Board can amend the By-Laws of the RISC-V foundation via a two-thirds affirmative vote. The Board appoints chairs of ad-hoc committees to address issues concerning RISC-V, and has the final vote of approval of the recommendation of the ad-hoc committees. All members of committees must be members of the RISC-V Foundation. Committee chairs must report to the Board, and committees are subject to termination if the Board decides a committee is not making satisfactory progress. Given the worldwide interest in RISC-V, the Board will appoint Chairs of Regional Committees to promote RISC-V development in local communities.
Classes of Membership

- **Platinum Sponsor** dues of US$25,000 per year
  - 10 complimentary registrations for RISC-V meetings during the year of membership and the most prominent and largest display of company logos in online and print materials for RISC-V
  - Platinum members are eligible for Board seat elections and to Chair Foundation Technical Committees, Marketing Committees and Sub-Committees

- **Gold Sponsor** dues of US$10,000 per year
  - 7 complimentary registrations for RISC-V meetings during the year of membership and prominent display of company logos in online and print materials for RISC-V
  - Gold Sponsor members are eligible to Chair Foundation Technical Committees, Marketing Committees and Sub-Committees

- **Silver Sponsor** dues of US$5,000 per year
  - 5 complimentary registrations for RISC-V meetings and for their logos to be displayed in RISC-V online and print materials

- **All Sponsor organizations** have one vote per open position in Board elections.

- **Auditor** dues of US$2,500 per year (non-voting)
  - 2 complimentary registrations for RISC-V meetings during the year of membership and for their names to be listed in online and print materials for RISC-V

- **Individual Member** dues of US$99 per year (non-voting)
Foundation Status

- Articles of Incorporation filed August, 2015
  - RISC-V Foundation Corporation is a legal, non-profit operating entity – 501(c)(6)
- 60 member companies have joined the Foundation
- Board of Directors formed in Q2, 2016
- Technical & Marketing Committees formed in Q3, 2016
  - Chairs & Vice-Chairs elected
- Membership Agreement & Bylaws ratified and released in Q4, 2016
RISC-V Foundation Board of Directors

- Krste Asanović, Chairman
  - Professor in the EECS Department at UC Berkeley
- Zvonimir Bandić
  - Senior Director of Next Generation Platform Technologies at Western Digital Corporation
- Charlie Hauck
  - CEO of Bluespec Inc.
- David Patterson
  - Retired Professor Computer Science UC Berkeley
- Jothy Rosenberg
  - Associate Director of the cyber security group at Draper Laboratories
- Frans Sijstermans
  - Vice President Engineering at NVIDIA
- Ted Speers
  - Technical Fellow, Head of Product Architecture for Microsemi’s SoC Group
RISC-V Technical Committee

- Chair Yunsup Lee, SiFive, Vice Chair Silviu Chiricescu, BAE Systems
- Currently consists of 9 task groups:
  - Opcode space management, Krste Asanovic, UC Berkeley
  - Privileged ISA specification, Andrew Waterman, SiFive
  - Formal specification, Rishiyur Nikhil, Bluespec
  - Debug specification, Megan Wachs, SiFive
  - Security, Joe Xie, NVIDIA
  - Vector extensions, Krste Asanovic, UC Berkeley
  - SW tool chain, Arun Thomas, BAE Systems
  - Bit Manipulation, Rex McCrary, AMD
  - Memory Consistency Model, Daniel Lusting, NVIDIA
RISC-V Marketing Committee

- Chair Arun Thomas, BAE Systems, Vice Chair Ted Marena, Microsemi
- Currently Consists of 5 Task Groups
  - RISC-V Content: Michael Gielda (AntMicro)
  - Workshops: Jack Kang (SiFive)
  - Industry Outreach: Neil Hand (Codasip), Dmitry Alenushkin (Syntacore)
  - Open Source and University Outreach: Arun Thomas (BAE Systems), Art Swift (Esperanto)
  - RISC-V 2020: Art Swift (Esperanto), Neil Hand (Codasip)

9 May 2017
RISC-V Foundation Summary

- Strong Industry Support
  - 60 member companies
  - Broad commercial and academic interest (sold out 6 straight workshops)

- RISC-V Chosen Best Technology of 2016 by The Linley Group

- Board of Directors formed in Q2 2016

- Technical & Marketing Committee Chairs & Vice-Chairs elected in Q3 2016

- 7th RISC-V Workshop save the date...
  - November 28th – 30th, 2017, Milpitas, California