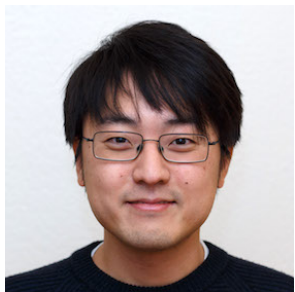




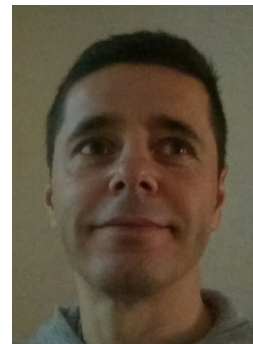
# Technical Committee Update



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# Technical Committee Goals

- Maintain a roadmap of the RISC-V ISA
- Coordinate effort on various ISA extensions and specifications
- Coordinate effort upstreaming software development tools (compiler, debugger, etc.)
- Establish processes to define and standardize ISA extensions
- Provide and maintain a set of compliance tests to ensure conformance with the evolving RISC-V ISA and its extensions
- Provide guidelines for platform integration to avoid fragmentation in the RISC-V software ecosystem
- Make sure RISC-V workshop has a great program!

# Technical Committee Task Groups

- Chair Yunsup Lee, SiFive, Vice Chair Silviu Chiricescu, BAE Systems
- Currently consists of 9 task groups:
  - Opcode space management, Krste Asanovic, UC Berkeley
  - Privileged ISA specification, Andrew Waterman, SiFive
  - Formal specification, Rishiyur Nikhil, Bluespec
  - Debug specification, Megan Wachs, SiFive
  - Memory Consistency Model, Daniel Lusting, NVIDIA
  - Security, Joe Xie, NVIDIA
  - Vector extension, Krste Asanovic, UC Berkeley
  - Bit Manipulation extension, Rex McCrary, AMD
  - SW tool chain, Arun Thomas, BAE Systems



# Technical Committee Highlights

- RISC-V officially supported in binutils 2.28 release
- RISC-V officially supported in GCC 7.1 release
- RISC-V privileged specification v1.10 published
  - <https://github.com/riscv/riscv-isa-manual>
- Debug specification v013 published
  - <https://github.com/riscv/riscv-debug-spec>
- Memory consistency model TG formed



- 1H 2017
  - RISC-V privileged spec draft v1.10 released
    - M-mode/S-mode changes must be backwards-compatible after this date
  - Calling convention & ELF format documented
    - <https://github.com/riscv/riscv-elf-psabi-doc>
- 2H 2017
  - RV32EMAC, RV32IMAFDQC, RV64IMAFDQC ratified
  - Debug spec ratified
  - Memory model spec proposal
  - Hypervisor spec proposal
  - Complete Unix platform spec proposal incl. hypervisor support

# Privileged ISA Spec TG

Talk today, TG Meeting on Thursday



- Charter
  - To define and specify a unified RISC-V privileged architecture and hardware platform
- Progress
  - Version 1.10 of supervisor-mode and machine-mode architecture have been proposed; no more backwards-incompatible changes
- Goals
  - Hypervisor architecture proposal by Sep '17
  - Complete Unix platform spec proposal, incl. hypervisor support, by Nov '17
  - Ratification end of '17/beginning of '18



## ■ Charter

- To produce a *formal* specification of the RISC-V ISA that
  - Implementation independent (no micro-arch details), high level, executable, suitable for mechanized formal tools
  - Readable
  - Complementary/in addition to the textual ISA spec docs
  - Compose seamlessly with Memory Model formal spec, which is focus of separate TG

## ■ Status

- Have just begun activities: 15 members
- Gathering resources (existing specs in L3, BSV and Coq)
- Discussing preferred styles, tools

# Debug Spec TG

Talk tomorrow, TG Meeting on Thursday



- Charter
  - To standardize HW debug for RISC-V cores
- Status
  - Version v013 spec allows for a variety of implementations
    - “Abstract” Interface for basic commands
    - Optional “Program Buffer” interface for arbitrary RISC-V Code
  - Bi-weekly meetings 8am PDT
- Goals
  - Ratification 2017



# Memory Model TG

Talk tomorrow, TG Meeting on Thursday



- Charter/Goals:
  - Build a rigorous and sound memory consistency model
  - Provide explanatory material as necessary
  - Follow the best modern practices of academia and industry
  - Ideally remain backwards-compatible, but not at the cost of ending up with a sub-standard memory model
- Status:
  - Task group formed mid-March and meets weekly
  - Many important tradeoffs still being debated
  - Hoping to get draft out within coming months

# Security TG

## TG Meeting on Thursday



- Charter
  - Define RISC-V security extension specification including:
    - RISC-V security model and assistant instructions
    - Crypto algorithm instructions (AES, SHA, RSA, ECC, Random)
- Status
  - Security extension 0.01 draft under review within TG
  - Crypto extension draft still working in progress
- Goals
  - Security and crypto extension 0.1 in next workshop



- Charter
  - Define RISC-V “V” standard extension
- Status
  - Roger Espasa, Esperanto joined as vice-chair
  - Members have been joining
  - Draft vector spec delayed due to work on priv arch and memory model
    - early text available in riscv-isa-manual repo
  - Begin regular meetings in June



- Charter
  - Define RISC-V “B” extension
- Status
  - Completed gathering proposals.
  - Implementing instructions to get good data on hardware costs.
    - Implementing different alternative designs where they exist
  - Created diagram of how instructions related to each other
    - Purpose: Objectively evaluate overlap to pick minimum number of instructions
  - Looking for vice-chair



- Charter:
  - To define a standard, easy to build and use software toolchain for the RISC-V ecosystem
- Updates:
  - Binutils 2.28 and GCC 7.1 now support RISC-V
  - FreeBSD 11.0 and Zephyr 1.7 support RISC-V
  - LLVM and gdb – initial set of patches have been submitted
  - Linux kernel and glibc – upstreaming will begin over the summer
  - QEMU - patches submitted for linux-user-mode
  - Continue to push on Linux distribution support
  - Full status: [RISC-V Software Status Wiki page](#)
  - ABI specification in progress

# Call for Participation

- All member organizations should nominate a person for the technical committee
- “J” extension TG looking for vice-chair
  - Chaired by David Chisnall (Cambridge)
- Compliance testing TG looking for participation
- Please let us know if you’d like to participate in a TG or start a TG
- Finally, thank you for your contribution!
- Any questions?