SCR1: open RISC-V compatible MCU core with support

Ekaterina Berezina
6th RISC-V Workshop
May 2017

www.syntacore.com
info@syntacore.com
Outline

- Company intro
- SCR1 overview
Executive summary

Announcing availability of the open-source SCR1 RISC-V MCU core

- **RV32I|E[MC] ISA**
  - Expected MCU uncore: IRQ controller, debug, bridges, scratchpad mem

- **Under permissive SHL (Solderpad Hardware License)**
  - Apache 2.0 derivative with HW specific

- [https://github.com/syntacore/scr1](https://github.com/syntacore/scr1)

Optional services provided:

- Support for core and tools
- Workload-specific customization
Syntacore introduction

IP company
Develops and licenses state-of-the-art RISC-V cores
- Initial line in available for evaluation
- SDKs, samples in silicon

Full service to specialize CPU IP for customer needs
- One-stop workload-specific customization
  - with tools/compiler support
- IP hardening at the required library node
- SoC integration and SW migration support
SCRx baseline cores

- **SCR1**: Minimalistic MCU-class open-source core
  - Minimal area configuration is <15 kGates

- **SCR3**: High-performance 32-bit MCU with privilege modes
  - Competitive characteristics

- **SCR4**: 32-bit MCU core with high-performance FPU
  - IEEE 754-2008 compatible

- **SCR5**: Efficient mid-range APU/embedded core
  - 1GHz@28nm, virtual memory, SMP support, Linux

Stable designs available for evaluation
- FPGA-based SDK, silicon samples by 2017

*Baseline cores: extensible and customizable*
SCR1 overview

MCU-class open-source core for deeply embedded applications and accelerator control

- SHL-licensed
- In System Verilog
- RV32I or RV32E base, optional M and C extensions
- M-mode only
- Integrated IRQ controller and advanced debug
- 32-bit AHB-lite external interface
- Optimized for area and power
- Customization/extensibility
SCR1 overview

- Configurable 2 to 4 stage in-order pipeline implementation
- Configurable high-performance or area-optimized multiply/divide unit
- Tightly coupled memory support
- Integrated Programmable Interrupt Controller
- Debug Controller with JTAG interface and HW Breakpoint support
SCR1 characteristics

- Minimal RV32EC config: **12 kGates***
- Balanced RV32IMC config: **28 kGates***
- Fmax: **250 MHz @ tsmc90lp***
  
  * tsmc.90nm.lp, op_cond: bc_wc -max tt_1p2v_25c

- Benchmarks

<table>
<thead>
<tr>
<th>Perf** per MHz</th>
<th>Coremark</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMIPS</td>
<td>-O2</td>
</tr>
<tr>
<td></td>
<td>-best**</td>
</tr>
<tr>
<td>Coremark</td>
<td>-O2</td>
</tr>
<tr>
<td></td>
<td>-best**</td>
</tr>
</tbody>
</table>

* Dhrystone 2.1, Coremark 1.0, GCC 5.2.0 BM from TCM
** O3-funroll-loops -fpeel-loops -fgcse-sm -fgcse-las -flto
SCR1 collateral

- Verification suite
  - testbench, tests, tracelog
- Documentation
- Basic simulation and synthesis env
- Reference designs
Why SCR1?

- Low risk/low effort RISC-V migration path
  - Start on your own with “plan B”
- Maintenance
  - Updates with the entire SCRx product line
- Customization option for 10x
- We encourage academic/educational use
Thank you!

https://github.com/syntacore/scr1

www.syntacore.com
info@syntacore.com