Achronix Speedcore

Risc-V Workgroup

May 8-11, 2017
Achronix Introduction

- Founded in 2004 at Cornell University.
- Initially developed high performance self-timed FPGAs.
- Currently in production:
  - Standalone FPGAs, FPGA Accelerator cards, and Embedded FPGAs.

Achronix has over 100 person-years invested in the ACE design tool suite.

San Jose, CA  
Bangalore, India
High-performance FPGA core, available to be added to your device.

- We work with your technology node, your metal stack.
- You control the FPGA size, BRAM, LRAM, and DSP Density, IO count, etc.

Deliverables Include

- GDSII, LEF files, LIB timing files, SPICE netlist, Power models, DFT Netlist, PI & SI simulation models, manufacturing vectors, characterization vectors, and extensive documentation.
- Custom version of the Achronix ACE tool suite
  - Includes synthesis, place-and-route, static timing analysis, debug tools, etc.
  - Supports your specific device.
High throughput, Low latency, Coherent, Programmable Acceleration

- An Achronix Speedcore IP with a 128b interface @ 600 MHz → **768 Gbps** with a round-trip latency of ~**10 ns**.
  - Compare to ~**100Gbps** effective throughput with ~**1200ns** latency for a PCIe Gen3x16 interface.
- Connect to the TileLink cache-coherent interconnect, allowing for **coherent** programmable acceleration.
  - Also supports AXI or other on-chip interfaces.
  - Multiple parallel interfaces for higher throughput.
- You control how many LUTs & Flops, DSP blocks, BRAM blocks, and LRAM blocks.
  - You can invent new block types to put in columns
- Speedcore can get it’s own L1 cache if the application would benefit.
Runtime-selection accelerator selection

- Switch between accelerator types as needed.
- Can bypass interface data and provide algorithm acceleration.
- Reconfiguration is ~2 ms per 100k LUTs.

IO Acceleration

- Accelerator fits between I/O & system interconnect.

- Support multiple of PCIe-based protocols
  - CCIX, CAPI, Thunderbolt

- Support programmable protocol extensions
  - Specialized transactions, Cache Coherency, Custom DMA Engine

- Programmable TCP/IP acceleration
  - Free up CPU cycles.

- Programmable packet inspection
  - Discard unsupported/suspicious packets before they use up memory & CPU bandwidth.
Achronix Speedcore eFPGA Compiler:
Fast Development of Customer Specific Speedcore IP

**Inputs**

**Deliverables**

**IP Deliverables:**
- GDSII
- Simulation files
- SI and PI models
- Test models
- Timing characterization
- Documentation

**Full Support in ACE Design Tools**
ACE Design Tools – high level feature overview

- Full Verilog, SystemVerilog and RTL support
- Full-fledged STA supporting CRPR, OCV derating, multiple corners
- TCL command language
- GUI and command-line control
- Highly efficient integrated data model
- Supports all current simulators
  - Synopsys VCS, Mentor QuestaSim, Aldec Riviera, Cadence Incisive.
- Linux and Windows support
- Protected/encrypted IP support

*Production Version 6.0.6 Available Now*
ACE Design Suite

Project Setup & Compile
ACE Design Suite
Floorplanning & Placement
Extensive Speedcore Documentation
Summary

- **Achronix**
  - is a profitable 12 year old company.
  - extensive experience designing, manufacturing, shipping, and supporting IP, devices, and boards.

- **Speedcore Embedded FPGA**
  - High-performance on-die programmability with extreme throughput, latency, and power improvements.
  - Tailored to each design: Size, RAM & DSP density, IO Count, Technology Node & metal stack, etc.

- **ACE**
  - Mature & full-featured FPGA design suite
  - Over 100 person-years of investment, used in hundreds of FPGA designs.
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