STATUS OF THE RISC-V MEMORY CONSISTENCY MODEL

Daniel Lustig
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NVIDIA
THE RISC-V MEMORY MODEL IS FINE!

• If you’re concerned about recent press, *don’t be!*
• We’re well aware of and on top of the issues
• We caught the spec bugs well before they’ll actually affect any implementations in practice
• Great example of the benefits of open-source ISA
MEMORY CONSISTENCY MODEL

The set of rules specifying the values that can be legally returned by memory loads
SEQUENTIAL CONSISTENCY

1. All threads are interleaved into a single “thread”
2. The interleaved thread respects each thread’s original instruction ordering (“program order”)
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For performance, most processors weaken rule #2
REORDERINGS ALLOWED BY RISC-V (AND OTHERS)

Sequential Consistency

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<tr>
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<tbody>
<tr>
<td>Ld</td>
<td>St</td>
</tr>
<tr>
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TSO (x86)

| Ld | — | ??? | St | — | — |

RISC-V

| Ld | — | — |
| St | — | — |

Power, ARM

“Y” = ordering enforced by default

“—” = ordering not enforced by default
**REORDERINGS ALLOWED BY RISC-V (AND OTHERS)**

This is a common presentation of memory models, but it’s a woefully incomplete picture!

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THE MODEL AS AN UPPER BOUND

Where should RISC-V draw the line?

Sequential Consistency
THE MODEL AS AN UPPER BOUND

Where should RISC-V draw the line?

Total Store Order (x86)

Sequential Consistency
Where should RISC-V draw the line?

THE MODEL AS AN UPPER BOUND

- Total Store Order (x86)
- Sequential Consistency
- ARM v8.2
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IBM Power

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WEAKENING EVEN FURTHER...

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WEAKENING EVEN FURTHER...

1. All threads are interleaved into a single “thread”
2. The interleaved thread respects each thread’s original instruction ordering (“program order”)
3. Loads return the value of the most recent store to the same address, according to (some other rules)

For performance, most processors weaken rule #2
Most weaken rule #1 as well
Q: Can I think of an execution as an interleaving of the instructions in each thread (in some order)?
STORE ATOMICITY

Q: Can I think of an execution as an interleaving of the instructions in each thread (in some order)?

A: No! That would make it illegal to forward values from a store buffer!

Because with a store buffer, cores can read their own writes “early”
STORE ATOMICITY

- Option 1: forbid store buffer forwarding, keep a simpler memory model, sacrifice performance
- Option 2: change the memory model to allow store buffer forwarding, at the cost of a more complex model
- Nearly all processors today choose #2
STORE ATOMICITY

• Q: Can I think of an execution as an interleaving of the instructions in each thread (in some order), with an exception for store buffer forwarding?
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A: Yes, on x86 and ARMv8.2

- simpler programming model

No, on IBM Power and GPUs

- more scalable; allows more HW optimizations
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x86 and ARMv8.2 are “(other-/weak-) multi-copy atomic”

IBM Power and GPUs are not multi-copy atomic
EXAMPLE: SIMULTANEOUS MULTITHREADING

- Consider the store buffer forwarding a store value from one thread to another
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**SIMULTANEOUS MULTITHREADING**

- Consider the store buffer forwarding a store value from one thread to another.
- Threads disagree about the order of events!
SIMULTANEOUS MULTITHREADING

Thread 0
In-Order CPU Core w/ SMT
Store Buffer
Memory

Thread 1
In-Order CPU Core w/ SMT
Store Buffer

Thread 2
In-Order CPU Core w/ SMT
Store Buffer

Thread 3

Store A happened before Store B

Store B happened before Store A

• Option 1: require architects to prevent cores from “reading others’ writes early”

• Option 2: require programmers to reason about the possibility that different threads see entirely different orderings
## PENDING/POSSIBLE CHANGES TO THE MODEL

<table>
<thead>
<tr>
<th>Feature</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-copy atomicity</td>
<td>Major debate!</td>
</tr>
<tr>
<td>Enforce same-address ordering (including load-load pairs)</td>
<td>Required!</td>
</tr>
<tr>
<td>Forbid load-store reordering (for accesses to different addresses)</td>
<td></td>
</tr>
<tr>
<td>Enforce ordering of address/control/data-dependent instructions</td>
<td>Still sorting out the details!</td>
</tr>
<tr>
<td>Which FENCE types? (.pr, .pw, .sr, .sw? Other?)</td>
<td></td>
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HOW DOES THE MODEL AFFECT YOU?

- **Programmers**: it doesn’t, unless you’re writing assembly
- **Compiler writers**: this is really important! Let’s talk!
- **Architects of simple cores/SoCs**: this shouldn’t affect you, but if you get more aggressive, check back in
- **Architects of high-performance cores/SoCs**: this will affect how aggressive you can be, and will determine how much complexity can/can’t get exposed beyond the ISA. Let’s talk!
IT’S ALWAYS SAFE TO BE CONSERVATIVE

- If your architecture is simple and conservative (in-order pipeline, simple memory design, etc.), it will be compliant with any model we’ll use
  - e.g., if the model chooses to allow non-atomicity, your implementation can still safely be multi-copy atomic
  - e.g., if you want to ignore the .pr, .pw, .sr, and .sw fence bits, and just always do a full fence, that’s fine too

- The memory model committee will publish more specific and concrete guidance
CONCLUSIONS

• RISC-V memory model details are still being worked out
  • Expected timeline: months, not years
• These details largely only affect more aggressive future implementations; today’s designs are unaffected
• Memory model committee will deliver spec + guidance
• If you’re considering an aggressive design, or just want to get clarification or more detail, come talk to us!
  
  dlustig@nvidia.com