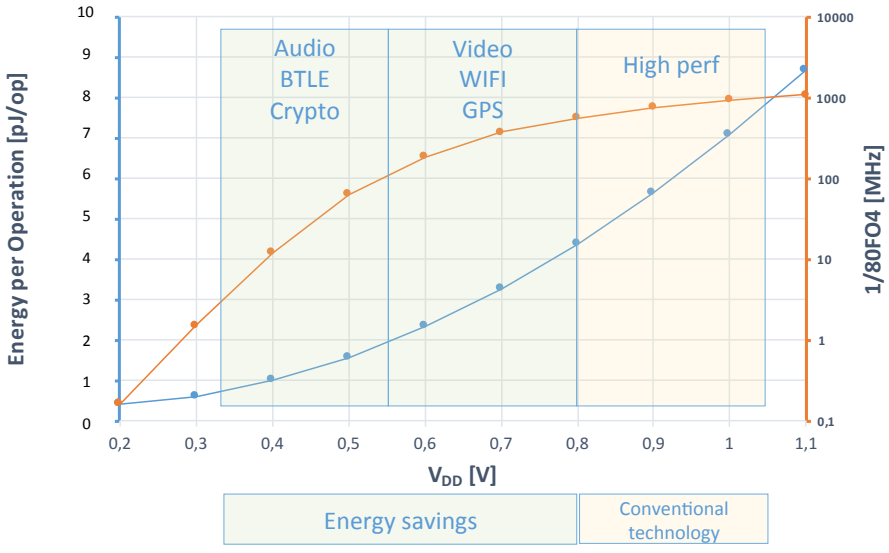
MINIMA PROCESSOR

~~28~~ 16 Microwatt RV32IMAC

RISC-V Workshop, Shanghai, 8.5.

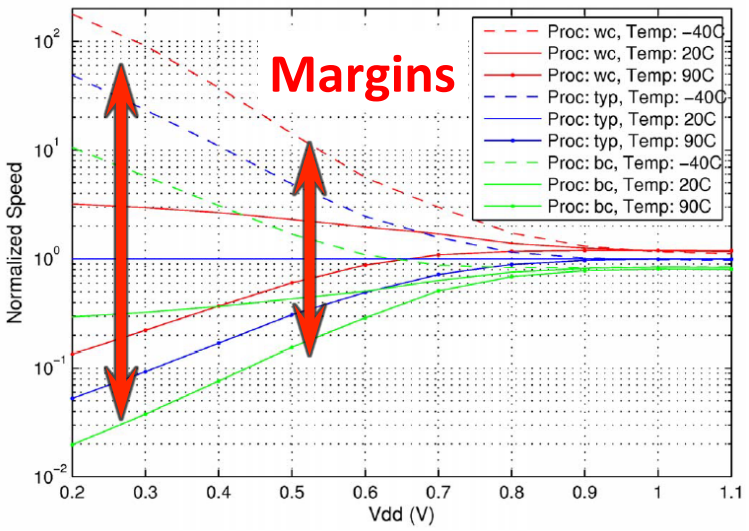
Why the buzz around Ultra-Low Voltage?



- Energy per operation optimum exists at 0.3-0.4V Vdd for modern silicon processes vs today's nominal Vdd of 1V
- Since $E = C*V^2$

⇒ Energy per Instruction at sub-threshold region can be 15x lower than at nominal Vdd

The Challenge



The Challenge – The Traditional "Solution"

Challenges of low-voltage design:

- Poor transistor and cell models
  - Neither transistor or digital cell libraries characterized for sub-threshold operation
- Large dependency on process and environment variation

Traditional "solutions":

I. For **every process**, detailed characterization of device and cell libraries needed
→ Slow, labor intensive

II. Or, do simple sanity check and add **a lot of margin** on the libraries
→ Lose a lot of the benefits to "sandbagging"

I. For every design, several validation and circuit synthesis rounds are needed
→ Multiple iterations, slow, labor intensive

II. Or, add a lot of timing margin at circuit synthesis
→ lose a lot of the attainable performance to "sandbagging"

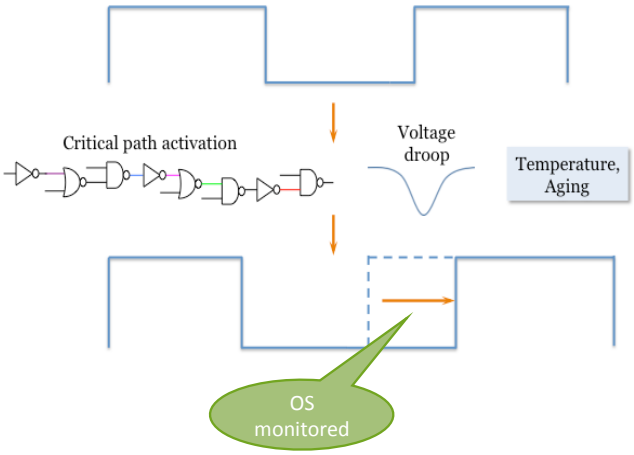
Instead of static margining Minima technology enables dynamic margining

The Minima Solution: Run-Time Margining

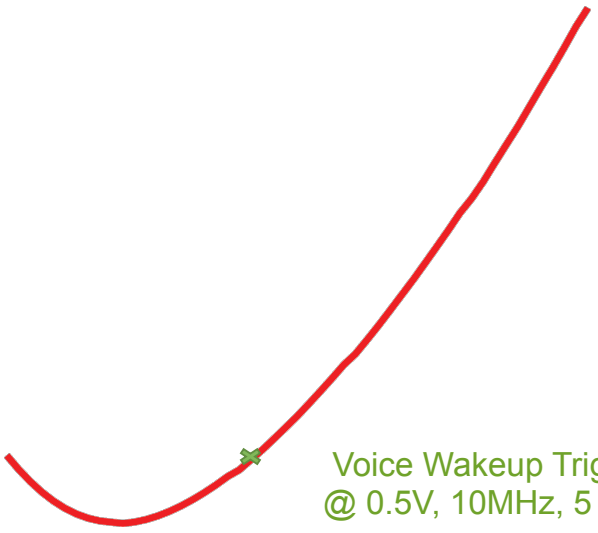
Real time adaptation to environment and process changes: Instead of worst case assumption, tune for best case / nominal operation

- Timing Event Processing (TEP) prevents real errors by dynamic feedback
  - Time borrowing + timing monitors
  - No need for microarchitectural error correction (e.g. out-of-order)
- System Monitor allows SW optimization and dynamic feedback
  - DVFS handles corners
  - OS controlled, Minima middleware

⇒Always operate at minimum energy for given task, data, ambient condition



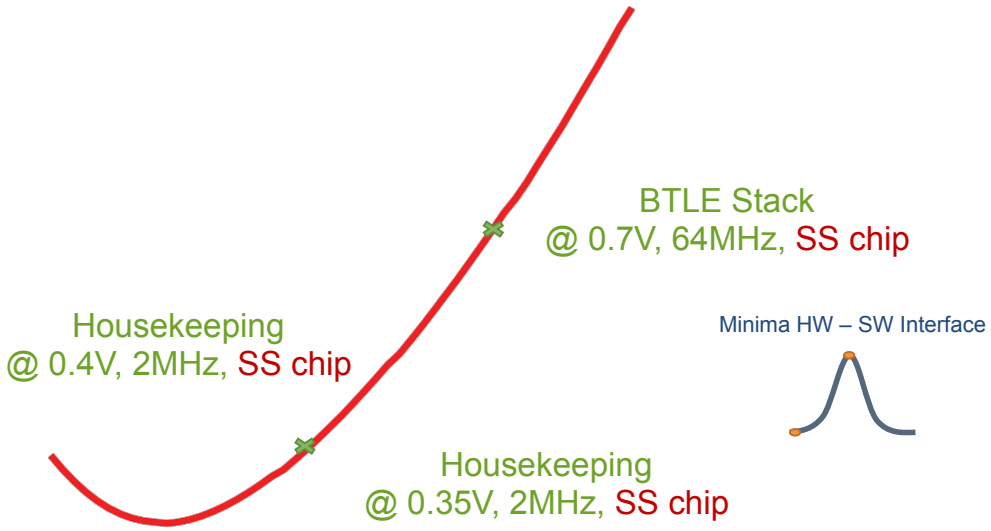
The Minima Solution: Ultra-Wide DVFS



Voice Wakeup Trigger2
@ 0.9V, 100MHz, 40 pJ/op

Voice Wakeup Trigger1
@ 0.5V, 10MHz, 5 pJ/op

The Minima Solution: Ultra-Wide DVFS



What Does Ultra-Low Voltage Mean for Your Datasheet?

Conditions		f_{HCLK}	Typ	Max(1)			Unit
				55 °C	85 °C	105 °C	
f_{HSE} = f_{HCLK} up to 16 MHz, included f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	270	400	400	400	µA
		2 MHz	470	600	600	600	
		4 MHz	890	1025	1025	1025	
	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	1	1.3	1.3	1.3	
		8 MHz	2	2.5	2.5	2.5	
		16 MHz	3.9	5	5	5	
		8 MHz	2.16	3	3	3	

2x higher difference

5-10x lower

RV32IMAC Post-Layout Results

VDD	Op Cond	Power	F_{max}
0.5V	TT, 25C	16µW	15
0.6V	WC, -40C	20µW	15
0.7V	TT, 25C	112µW	50
0.9V	TT, 25C	687µW	90
ISA: RV32IMAC, ICACHE: 4kB 2-way, Data scratchpad: 256kB			

Final Words: Rethink the System Level

- Radio energy: 100 nJ/bit (Zigbee), 50.00 nJ/bit (BT), 3.70 nJ/bit (Wifi)
- Memory energy: ~100pJ
  - Local memory accesses, DRAM accesses
  - Flash much more
- Basic compute @$VDD_{Nominal}$: ~50pj
- Basic compute @ULV: ~5pj
- Memory compression becomes cheaper in terms of energy
- Edge computing (contextual computing, fog computing, etc.) becomes cheaper in terms of energy
- The Minima IP portfolio (RISC-V, Audio DSP, Telecom DSP) will be rolled out during 2017

Acknowledgements Ali M. Niknejad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