Lauterbach Debug Support for RISC-V

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LAUTERBACH
DEVELOPMENT TOOLS

Leading Manufacturer of Microprocessor Development Tools

- Founded in 1979 by Lothar Lauterbach
- Headquarters in Hoehenkirchen, Germany (nearby Munich)
- Branch offices in China (3), France, Italy, Japan, Tunisia, UK and USA (2)
- Approximately 120 employees worldwide
- International well-established company

Our Strengths

- Technical know-how at highest level
  - HW and SW debug tools is all we do.
  - All design, development and manufacture in Munich
- Complete tool range for test and quality assurance of embedded designs
  - Chip/board bring-up
  - Driver/Bios Debug and Development
  - OS Debug and Development
  - Application Debug and Development
- Widest range of supported microprocessors in the market
  - Including SOC with dissimilar architectures
- Very early support for new processor architectures
- Protection of investments through modular system concept
- Long-standing relationships with customers and tool partners

Market Position

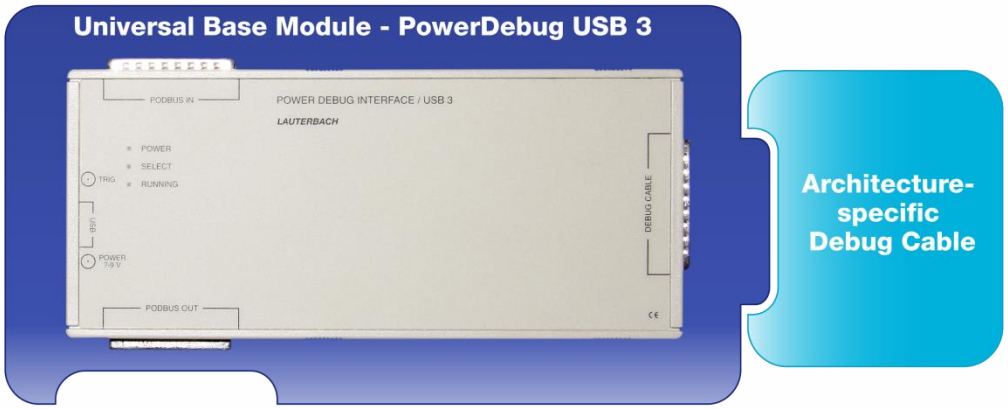
- Installed Lauterbach debuggers more than 100 000
- Market share worldwide > 40 %

No. 1 worldwide in JTAG debuggers

PowerDebug USB 3

Standard In-Circuit Debugger

- USB 3.0 interface to all hosts
- Supports for all microprocessor architectures
- Universal debug module, *connect to target via architecture-dependent debug cables*
- PODBUS interface to Logic Analyzer modules



PowerDebug PRO

High-Speed In-Circuit Debugger

- USB 3.0 or Gigabit Ethernet Interface to all hosts
- Universal debug module, *connect to target via debug cables*
- Extendable to add trace modules*
- Extendable to add logic analyzer modules

* Dependent on future support for RISC-V off-chip trace support

ARCHITECTURE SPECIFIC DEBUG CABLE

LA-2717 JTAG Debugger for RISC-V

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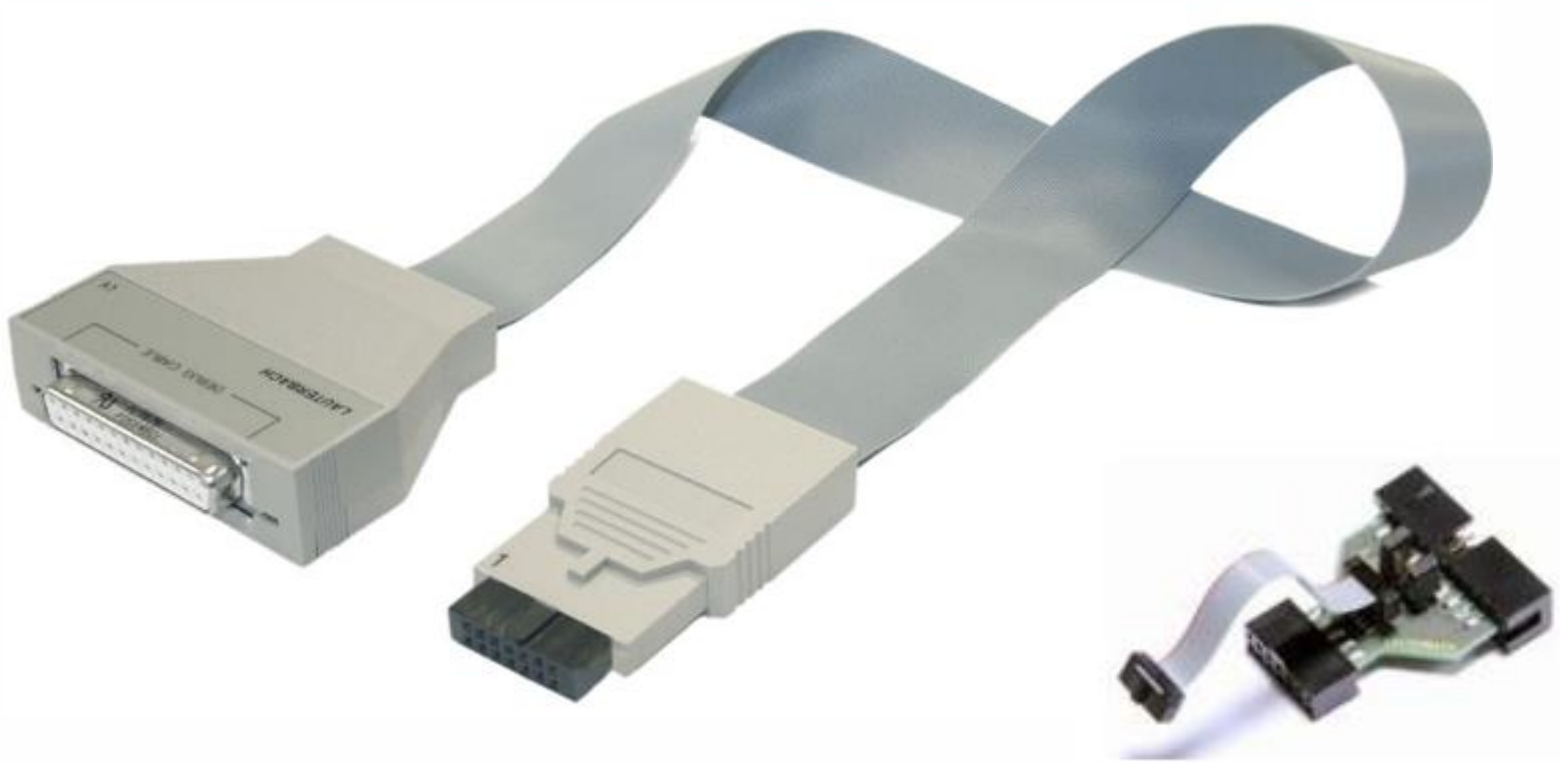
ARCHITECTURE SPECIFIC DEBUG CABLE

LA-2717 JTAG Debugger for RISC-V



LA-3863 ARM 20 to RISC-V 10

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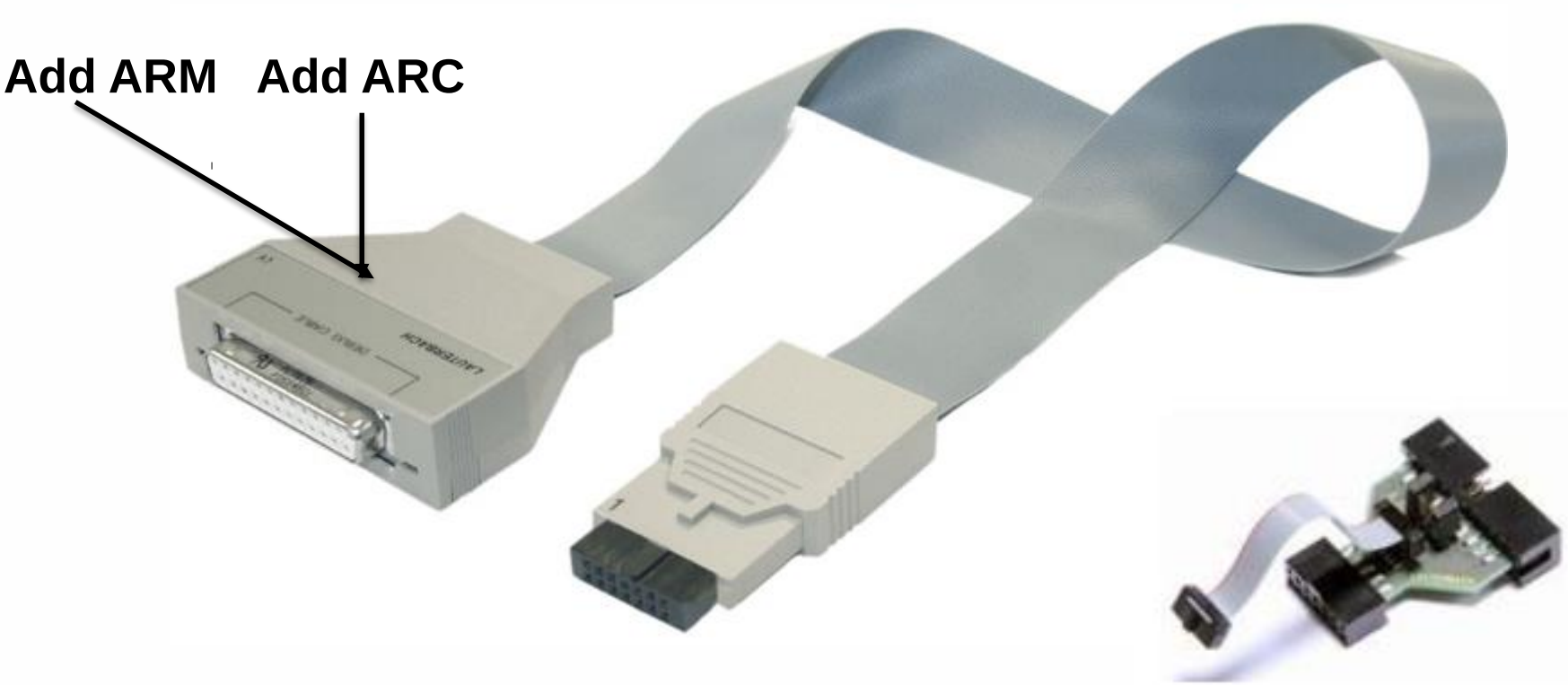

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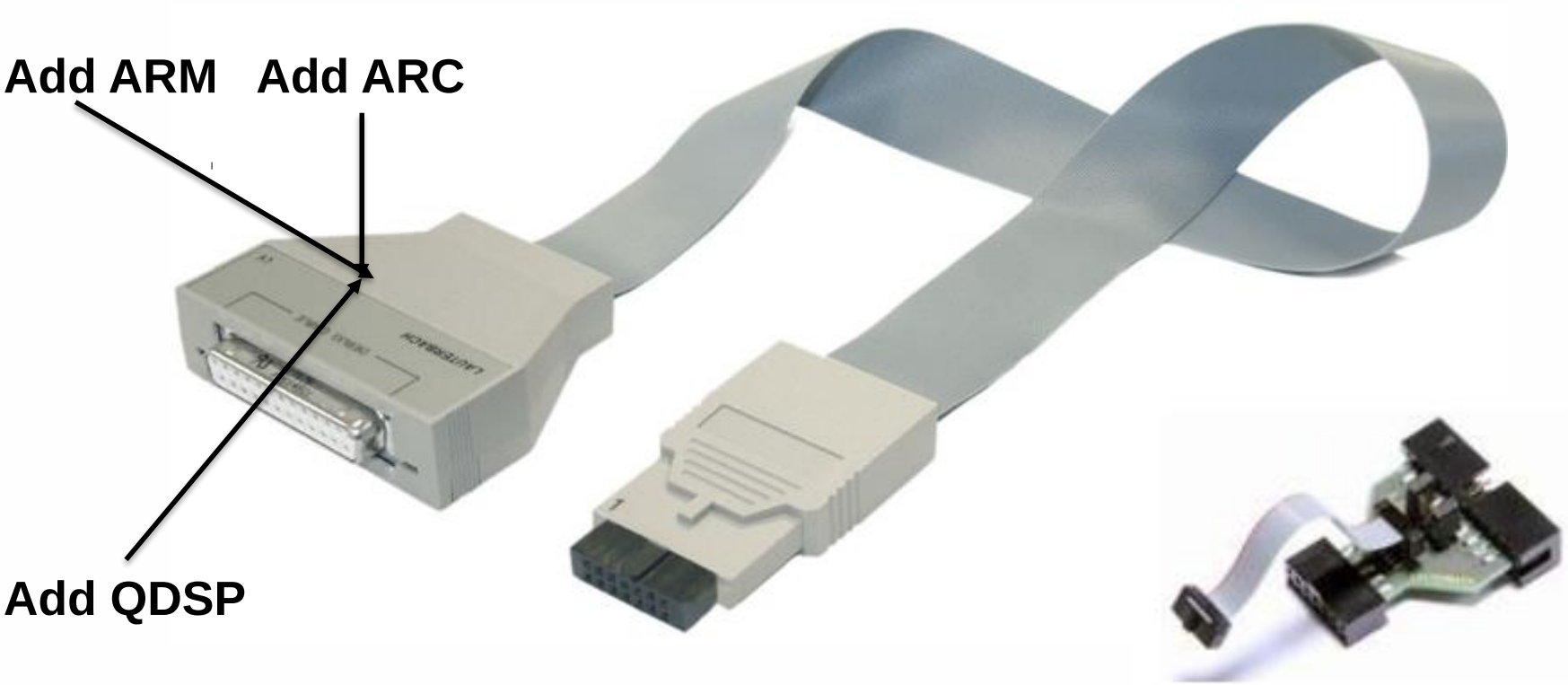

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ARCHITECTURE SPECIFIC DEBUG CABLE

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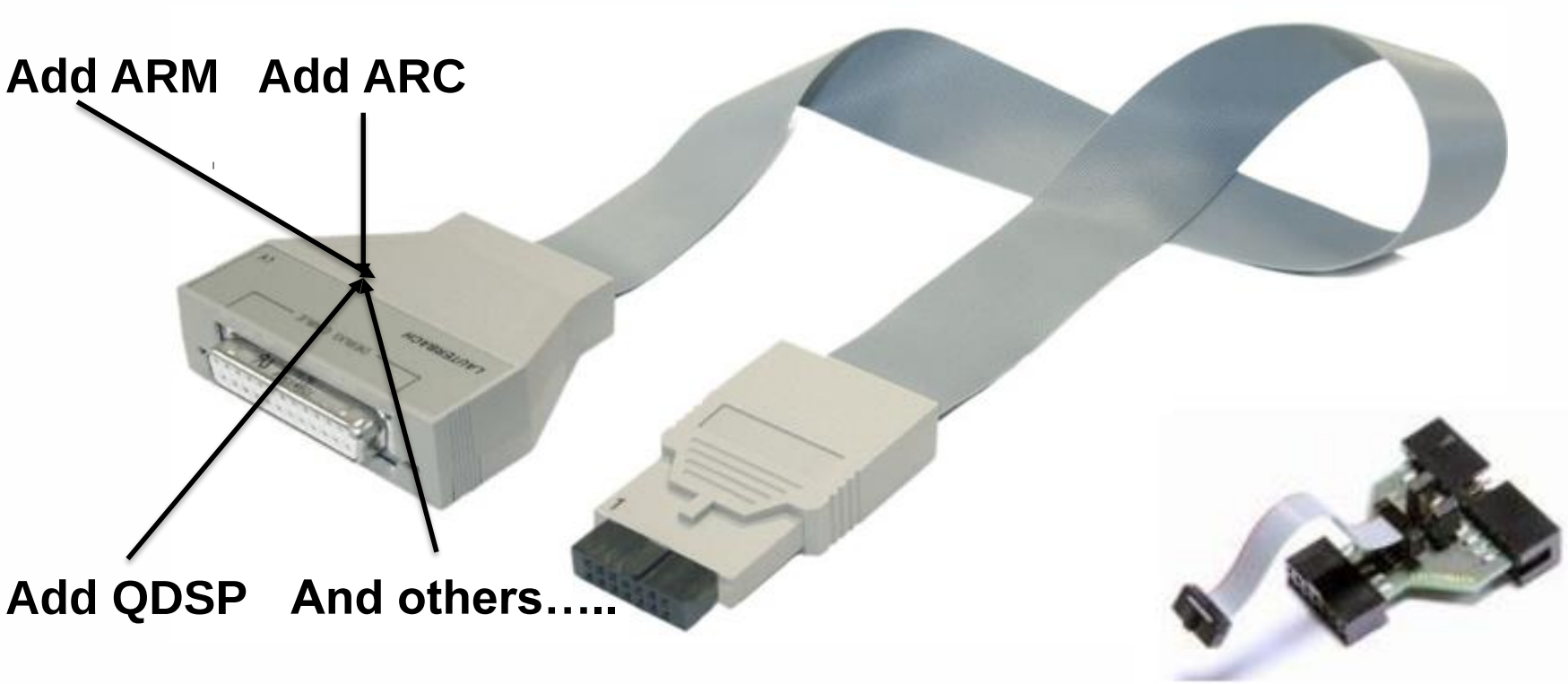

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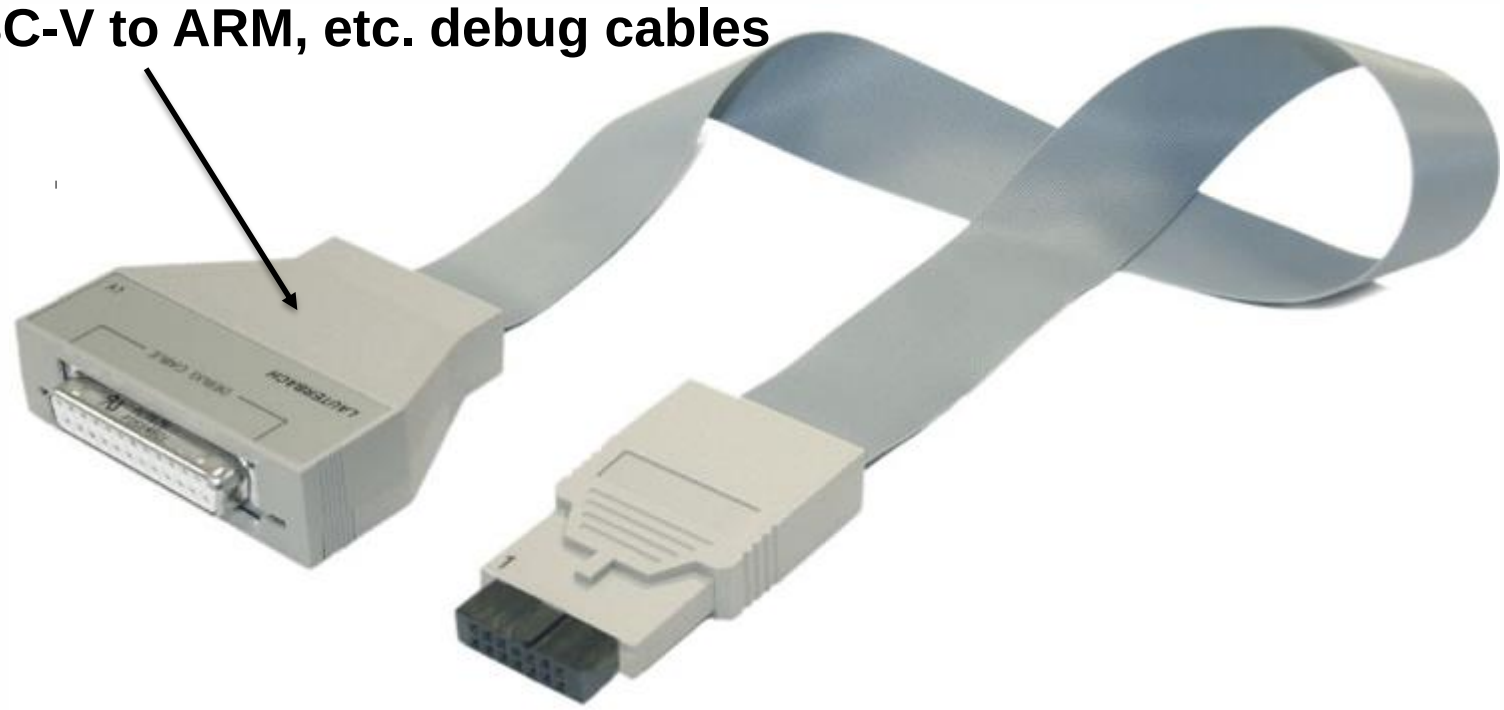
ARCHITECTURE SPECIFIC DEBUG CABLE

LA-2717A JTAG Debug Addition for RISC-V

ARCHITECTURE SPECIFIC DEBUG CABLE

LA-2717A JTAG Debug Addition for RISC-V

Add RISC-V to ARM, etc. debug cables



Tool Chain

- TRACE32 is one part of a complete tool chain that the developers use for their embedded design.
- TRACE32 PowerView provides an open interface for easy integration with:
  - Host platforms
  - Model-based designs
  - Compilers
  - Target OSs
  - Simulators, virtual prototypes and target servers

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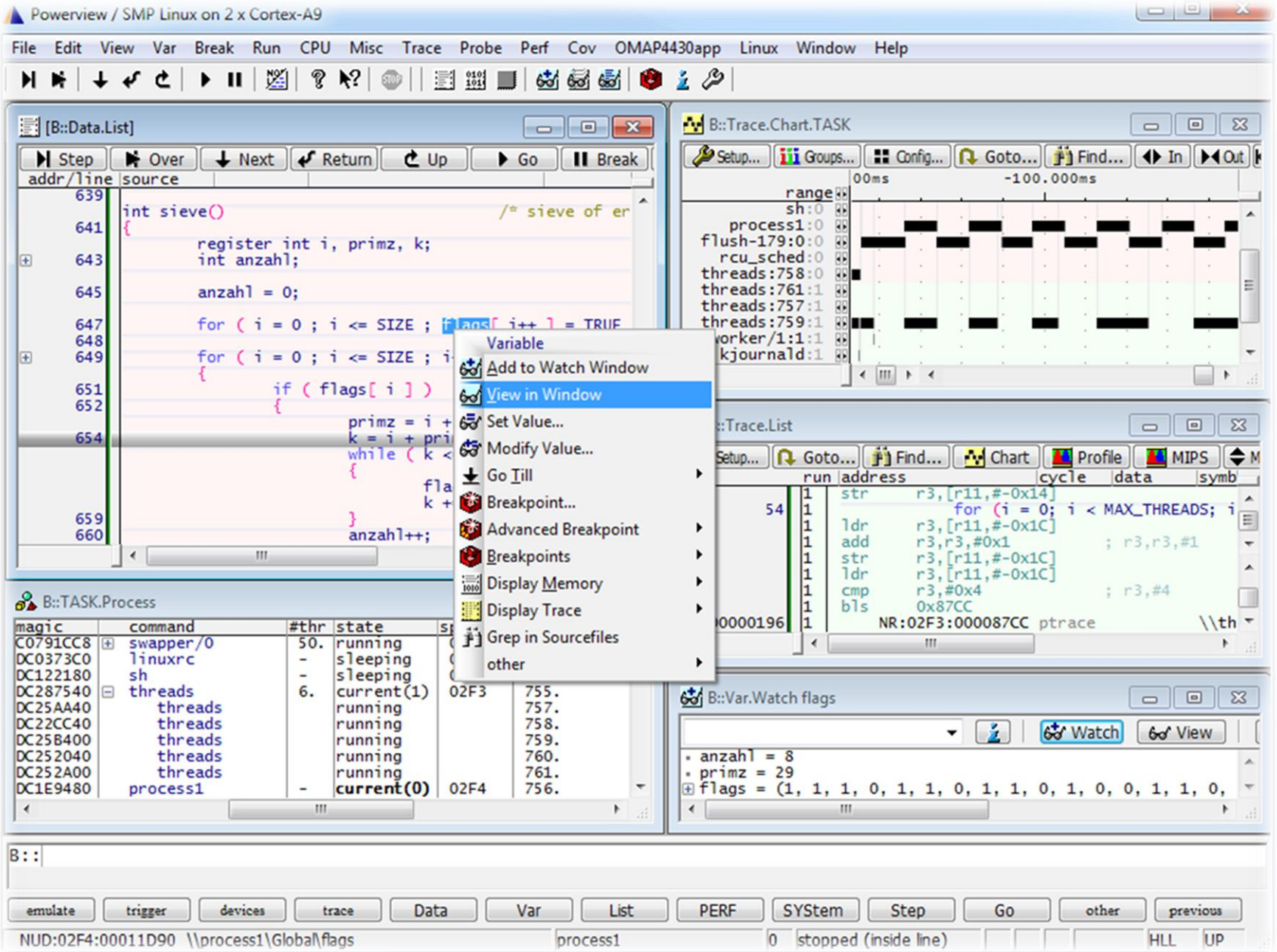
TRACE32 PowerView – the Uniform GUI for all Products



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TRACE32 Debugger

- Startup: Debug from reset vector or attach to target without altering its state
- Load program (e.g. ELF file) into target memory and extract debug information
- View program code in disassembled format or in high level language
- View call stack and local variables
- Assembler stepping, high level stepping
- Software breakpoints
- Common environment for HW debug or Instruction set simulator debug
- View and edit GPRs, program counter, floating point registers, CPU registers etc.
- View and edit memory (via CPU access or via system bus)
- Display current CPU state (running, stopped by SW breakpoint, stopped by HW breakpoint)
- Flash Programming
- Multicore debugging in SMP/AMP scenarios

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TRACE32 for RISC-V

- Run-control debugging via abstract commands and debug program buffer
- Support RV32 and RV64 ISA
- Hardware instructions and data breakpoints (match control trigger)
- Support standard JTAG interface (JTAG Debug Transport Module)
- Support standard ISA extensions: compressed instructions, floating point, …
- Roadmap includes:
  - Trace
  - Linux / Target OS awareness

COMPANY PROFILE

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http://www.lauterbach.com/bdmriscv.html

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LEADING through Technology

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Chip

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RISC-V Debugger

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- RISC-V Ecosystem
- Adaption
- TRACE32 Debug Features
- Details and Configurations

Highlights

- Support for JTAG interface (JTAG Debug Transport Module)
- Multicore debugging
- Debug from reset vector or attach to target without altering its state
- Run-control debugging via abstract commands and debug program buffer
- Support RV32 and RV64 ISA
- Support standard ISA extensions: compressed instructions, floating point, etc.
- Flash programming
- Easy high-level and assembler debugging
- Unlimited number of software breakpoints
- Onchip breakpoints on instructions and data (match control trigger)
- Display of configuration registers and peripherals at a logical level
- Target OS awareness
- Script language and API interface
- Support for SIFIVE E31

Operation Voltage | Order Information | Technical Support

Current RISC-V Release and Roadmap

- **Supported Target Architectures and Boards:**
  - Support RV32 and RV64 ISA
  - Board support for initial release: SiFive Coreplex E31 (RV32) and E51 (RV64)
- **Roadmap:**
  - Multicore debugging
  - Trace (as suitable solutions come available)
  - Additional target boards
  - Additional Debug Transport Modules

Thank you

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