Power Matters.™

Microsemi

Open Source RTOS Ports on RISC-V

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Open Source RTOS Ports on RISC-V

- Motivation
  - Various application domains – Industrial, IoT, Military, Space
  - Bare metal to large scale applications including networking stacks
  - Resource constrained environment
  - Create infrastructure to support variety of applications on RISC-V processors

- Infrastructure
  - Multiple open source RTOS support
  - Software development and debugging tools
  - Firmware and example applications

Open Source RTOS Ports on RISC-V

- FreeRTOS:
  - http://www.freertos.org/
  - Modified GNU General Public License

- Mynewt:
  - https://mynewt.apache.org/
  - Apache License, version 2.0

- Huawei LiteOS:
  - https://github.com/LITEOS
  - Open Source License

FreeRTOS

- **Features**
  - Popular cross-platform RTOS
  - Prioritized preemptive scheduling with time-slicing
  - Tick-less mode of operation
  - Idle task hook for applications
  - SafeRTOS – Certified version of FreeRTOS for safety critical applications
  - No BSP/HAL
  - Requires third party network protocols

- **Port**
  - 32bit: Running on RISC-V Soft Processor
  - 64bit: Running on Spike emulator

- **Next steps**
  - Publish as contributed port
  - Work towards distributing it as official port

Mynewt

- **Features**
  - Wireless stacks NimBLE, Bluetooth mesh, WiFi and more
  - IoT protocols e.g. CoAP
  - Secure bootloader to verify firmware integrity and authenticity
  - Power management
  - Cross-platform, well defined HAL and BSP
  - Package management and build using Newt tool
  - https://mynewt.apache.org/
  - Need to get familiar with Newt configuration and build tool

- **Port**
  - BSP support
  - MCU/HAL support
    - UART, GPIO

- **Next steps**
  - Create application with networking stack
  - Upstream the MCU and BSP port

Huawei LiteOS

- **Features**
  - Lightweight RTOS for IoT
  - Multiple toolchain support
  - Well defined project structure and HAL
  - Test suite for kernel features
  - Wireless networks, IoT gateway, home gateway
  - Ocean Connect IoT Platform(PaaS)
  - www.huawei.com/liteos
  - Less Documentation/porting guide for new architectures
  - Need for run-time statistics and task trace/debug support.

- **Port**
  - LiteOS Kernel port to RISC-V
  - BSP and HAL support
    - UART, GPIO, WiFi (esp8266)

- **Next Steps**
  - Port already pulled into LiteOS GitHub
  - Collaborate With Huawei

LiteOS Port

- **Kernel Port for a new ISA**
  - Context frame - TSK_CONTEXT_S
  - Context switching - los_dispatch_gcc.S
  - Interrupt handling functions
    - Interrupt lock, unlock, enable, disable functions
  - Memory model
  - Startup code

- **BSP and HAL port**
  - Board specific code e.g. memory, clock
  - Port device drivers in the HAL framework

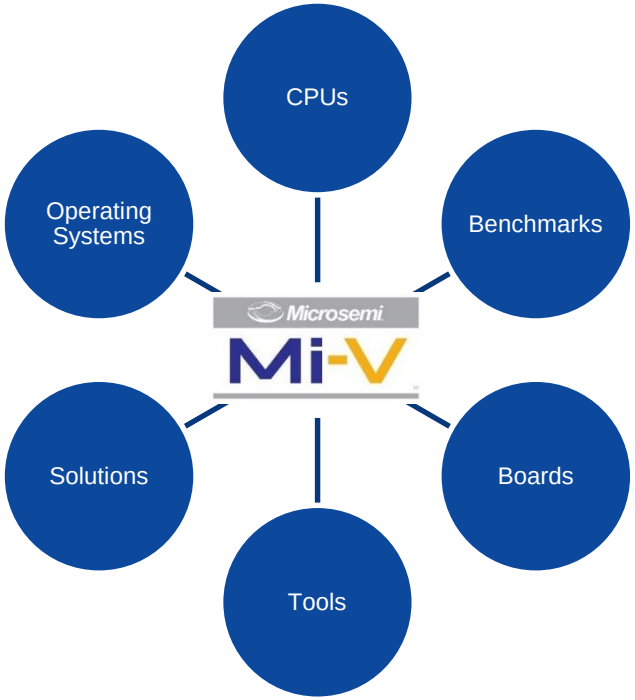
```
Software_IRQHandler:
    li      t0, 0x08
    csrrc   zero, mstatus, t0

    la      t0, g_pfnTskSwitchHook
    lw      t1, 0x0(t0)
    beqz    t1, TaskSwitch

TaskSwitch:
    la      t0, g_stLosTask
    lw      t1, 0(t0)
    sw      a2, 0(t1)

//Clear the task running bit of pstRunTask.
    la      t0, g_stLosTask
    lw      t1, (t0)
    lb      t2, 0x4(t1)
    andi    t2, t2, OS_TASK_STATUS_NOT_RUNNING
    sb      t2, 0x4(t1)

//copy pstNewTask into pstRunTask
    la      t0, g_stLosTask
    lw      t1, 0x4(t0)
    sw      t1, 0x0(t0)

//set the task running bit=1
    lh      t2, 0x4(t1)
    ori     t2, t2, OS_TASK_STATUS_RUNNING
    sh      t2, 0x4(t1)

//retireve stack pointer
    lw      sp, (t1)
```

RISC-V experience

- RISC-V ISA
  - Easy for assembly programing
    - Small ISA specification document.
    - Fewer addressing modes
    - zero register (x0)
  - RV32I context frame – 31 registers
    - RV32E extension (15 registers) is desired for deeply embedded applications
  - Absence of multiple register load/store instruction
  - Software interrupt for implementing context switch
- Privilege spec implementation
  - Soft reset – may be required in some cases such as reset after remote firmware upgrade.

Mi-V Ecosystem

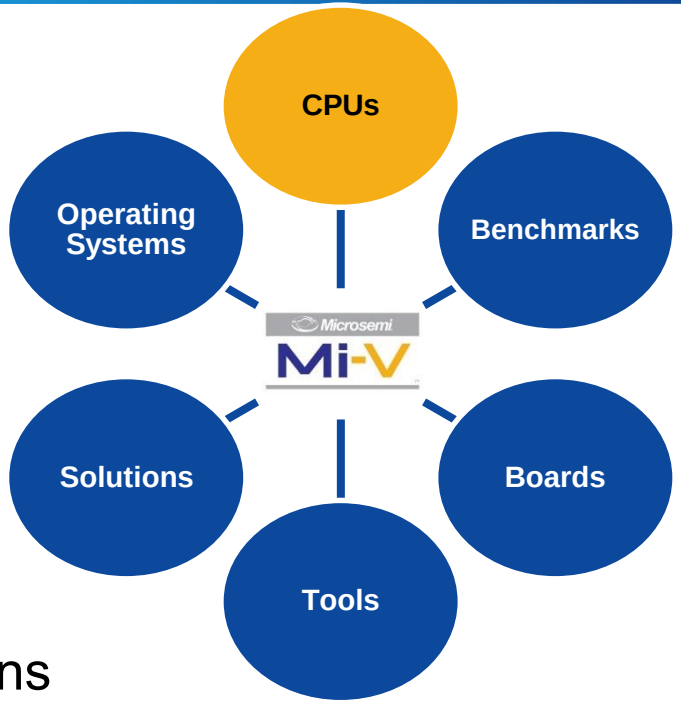
- A comprehensive offering to ease the adoption of RISC-V
- Open. Lowest Power. Programmable RISC-V Solutions.



Mi-V is the Microsemi RISC-V Ecosystem

Mi-V Soft Processors on Microsemi FPGA

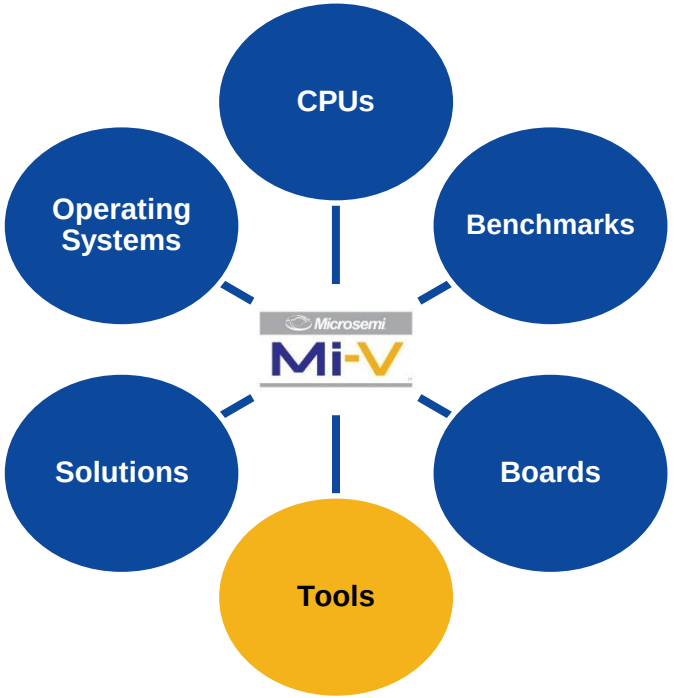
- Mi-V Soft Processors
  - MiV_RV32IMA_L1_AHB
  - MiV_RV32IMAF_L1_AHB



- Features
  - Based on Rocket Chip
  - Provides a single hardware thread (*hart*)
  - Machine-mode privileged architecture
  - RV32I Base ISA with ‘M’, ‘A’ and ‘F’ extensions
  - Integrated 8Kbytes instructions cache and 8Kbytes data cache
  - Two external AHB interfaces for IO and memory
  - Support up to 31 programmable interrupts
  - Debug unit with a JTAG interface
  - Best suited for low-mid range microcontroller applications

SoftConsole

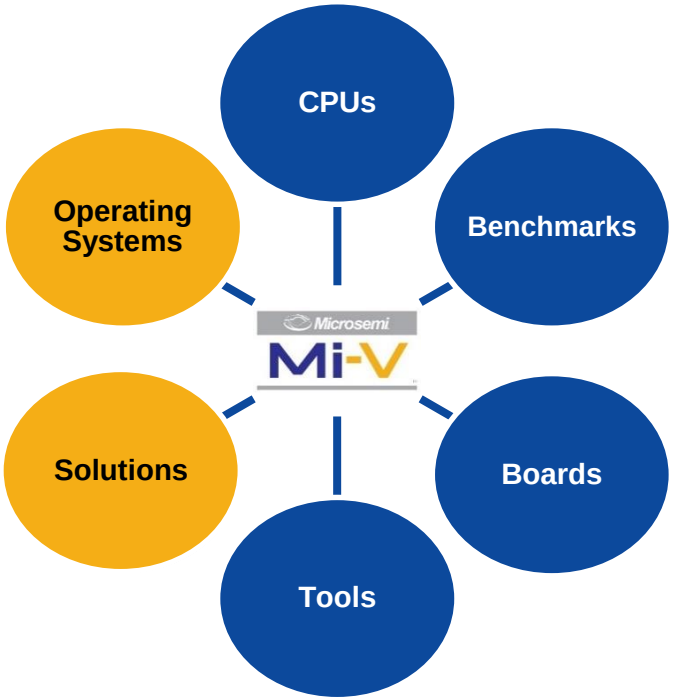
- Eclipse based IDE for software development
  - Supported platforms
    - Windows
    - Linux
  - Supported CPUs
    - Mi-V
    - ARM Cortex-M (M1, M3)
  - Supported JTAG programmers
    - FlashPro5
    - Olimex
    - Any programmer supported by openocd
  - Free Download
    - https://www.microsemi.com/products/fpga-soc/design-resources/design-software/softconsole



Mi-V RTOS Support and Solutions

- Ready to run example projects
- SoftConsole example projects should run on any (ideally) RV32I platform.
  - Verified on Mi-V and HiFive1
- Plans to enhance and maintain the RTOS ports

- FreeRTOS
  - https://github.com/RISCV-on-Microsemi-FPGA/FreeRTOS
- Mynewt
  - https://github.com/RISCV-on-Microsemi-FPGA/MyNewt
- LiteOS
  - https://github.com/RISCV-on-Microsemi-FPGA/LiteOS



Thank You

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