Strong Formal Verification for RISC-V

From Instruction-Set Manual to RTL

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MIT CSAIL
RISC-V Workshop
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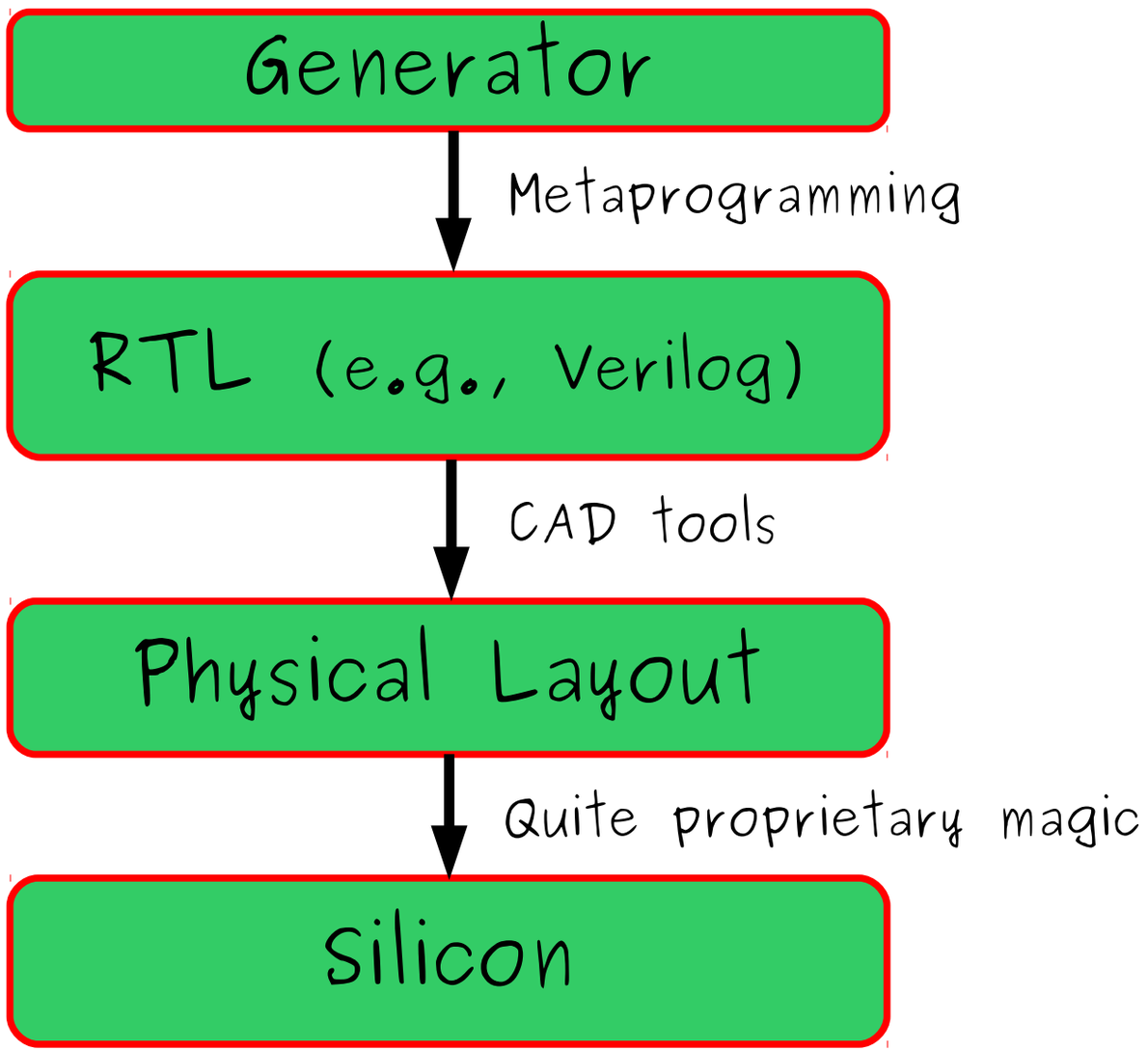
Joint work with: Arvind, Thomas Bourgeat, Joonwon Choi, Ian Clester, Samuel Duchovni, Jamey Hicks, Muralidaran Vijayaraghavan, Andrew Wright

A Cartoon View of Digital Hardware Design



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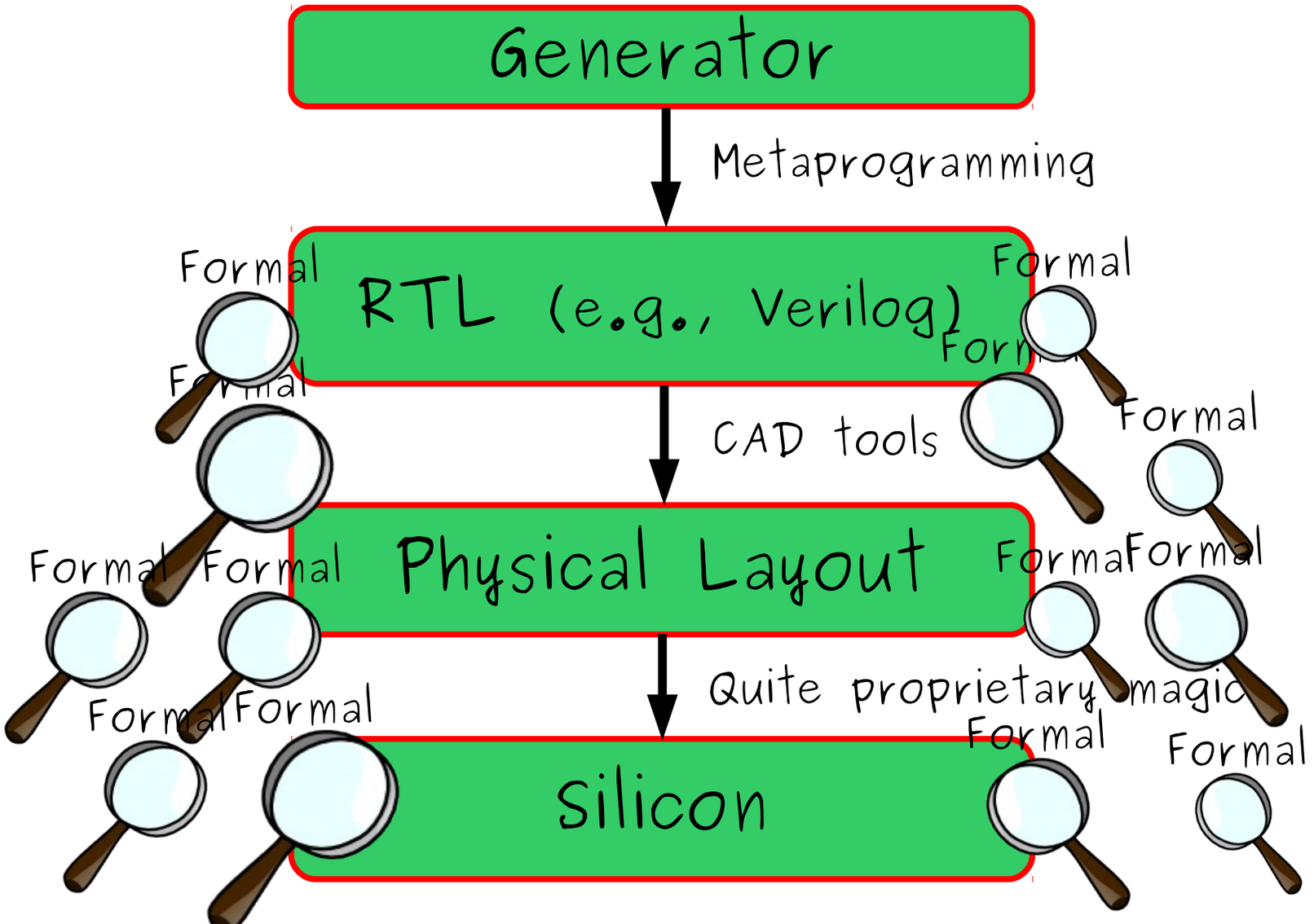
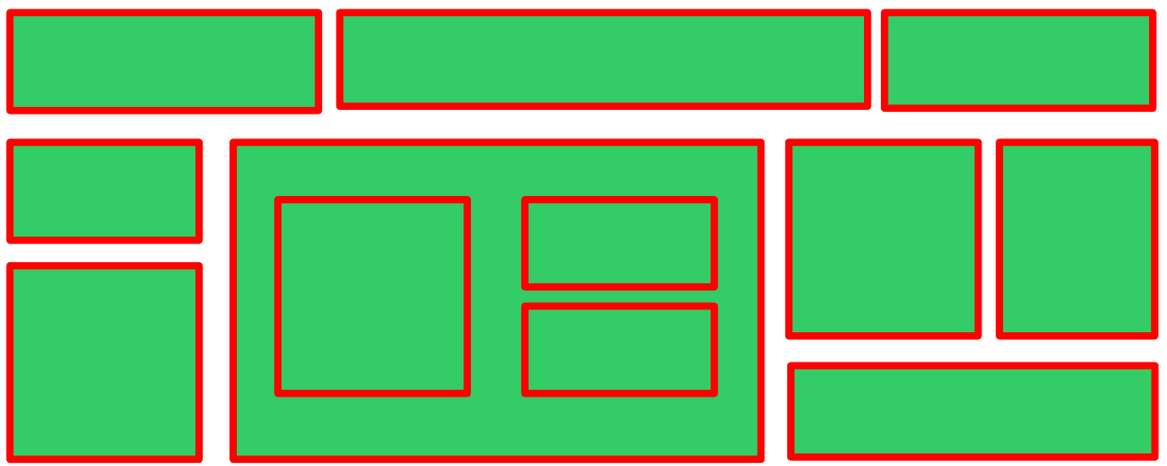


Simplification #1: Prove a Shallow Property



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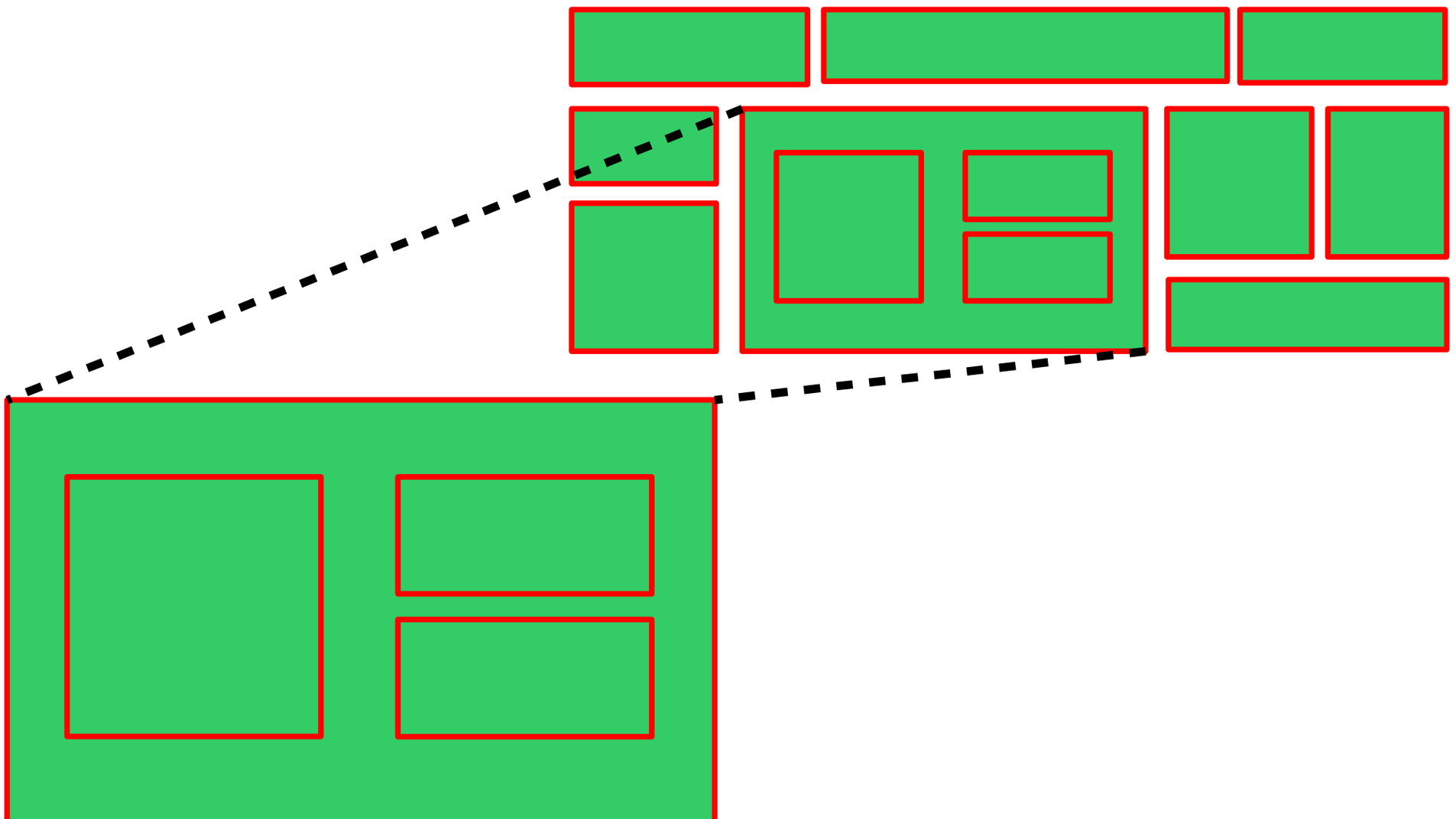

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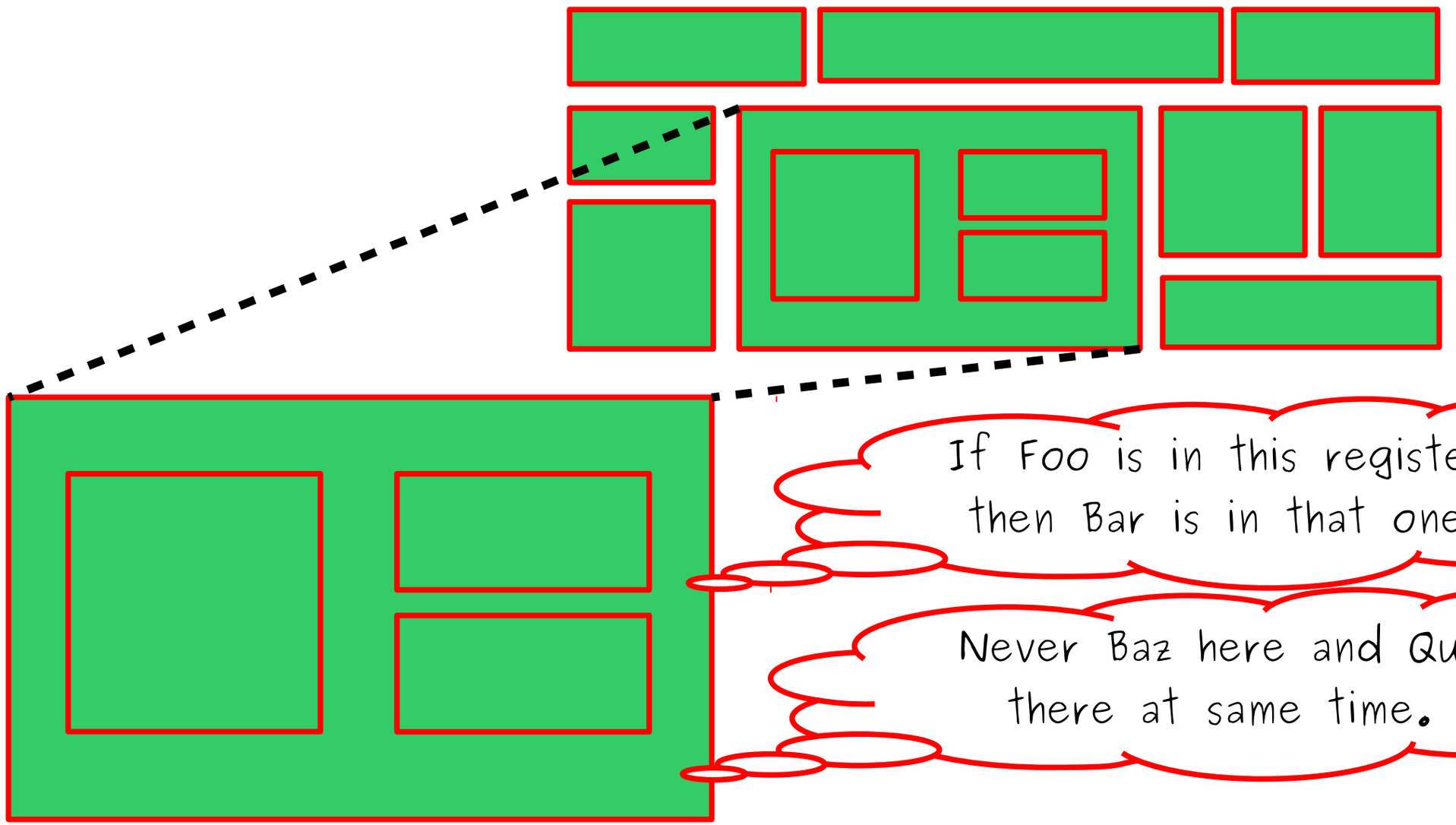

Common practice: prove some

Invariants

If Foo is in this register, then Bar is in that one.

Never Baz here and Qux there at same time.

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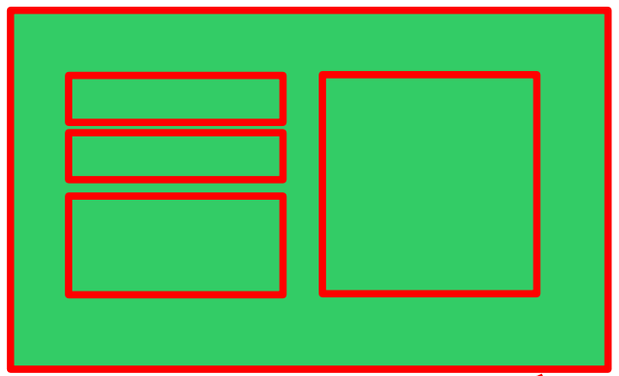
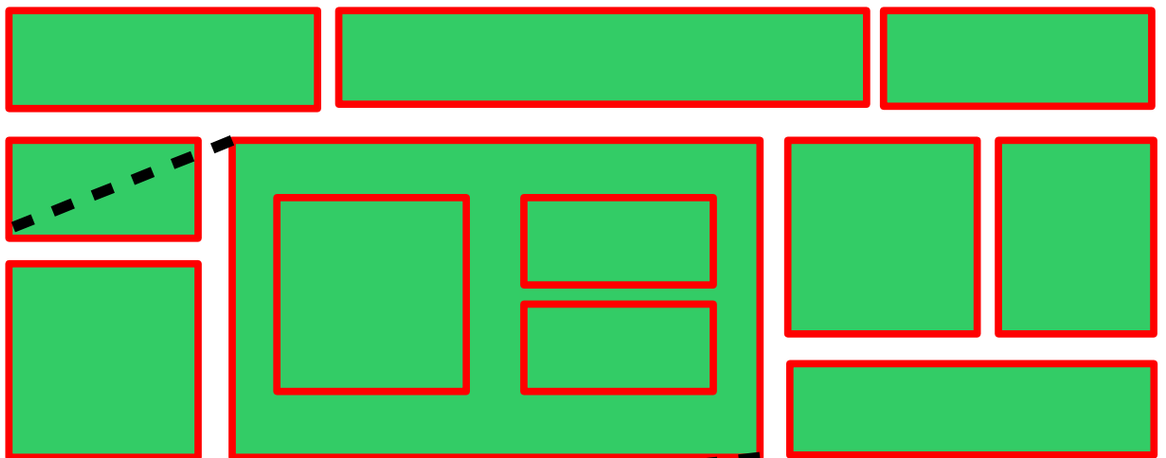
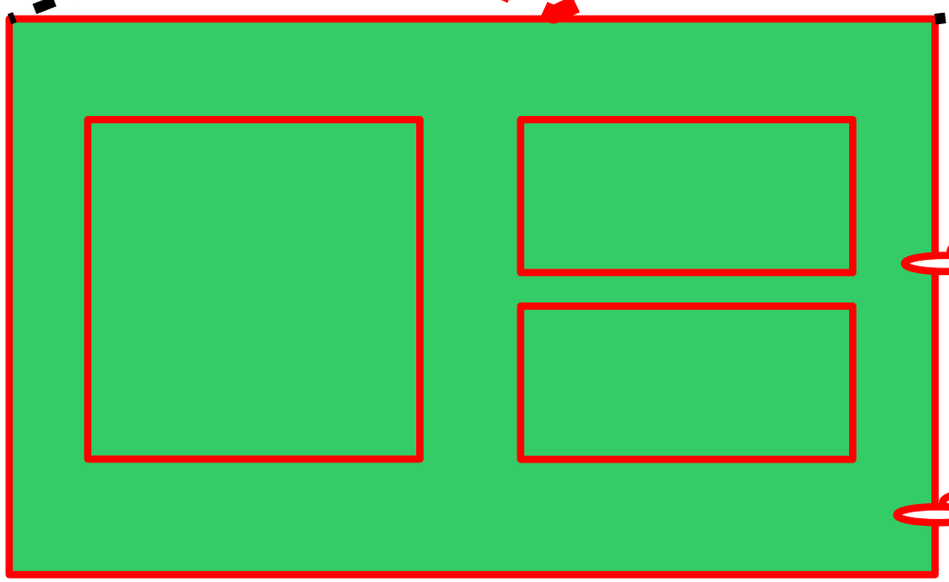




or Boolean equivalence check



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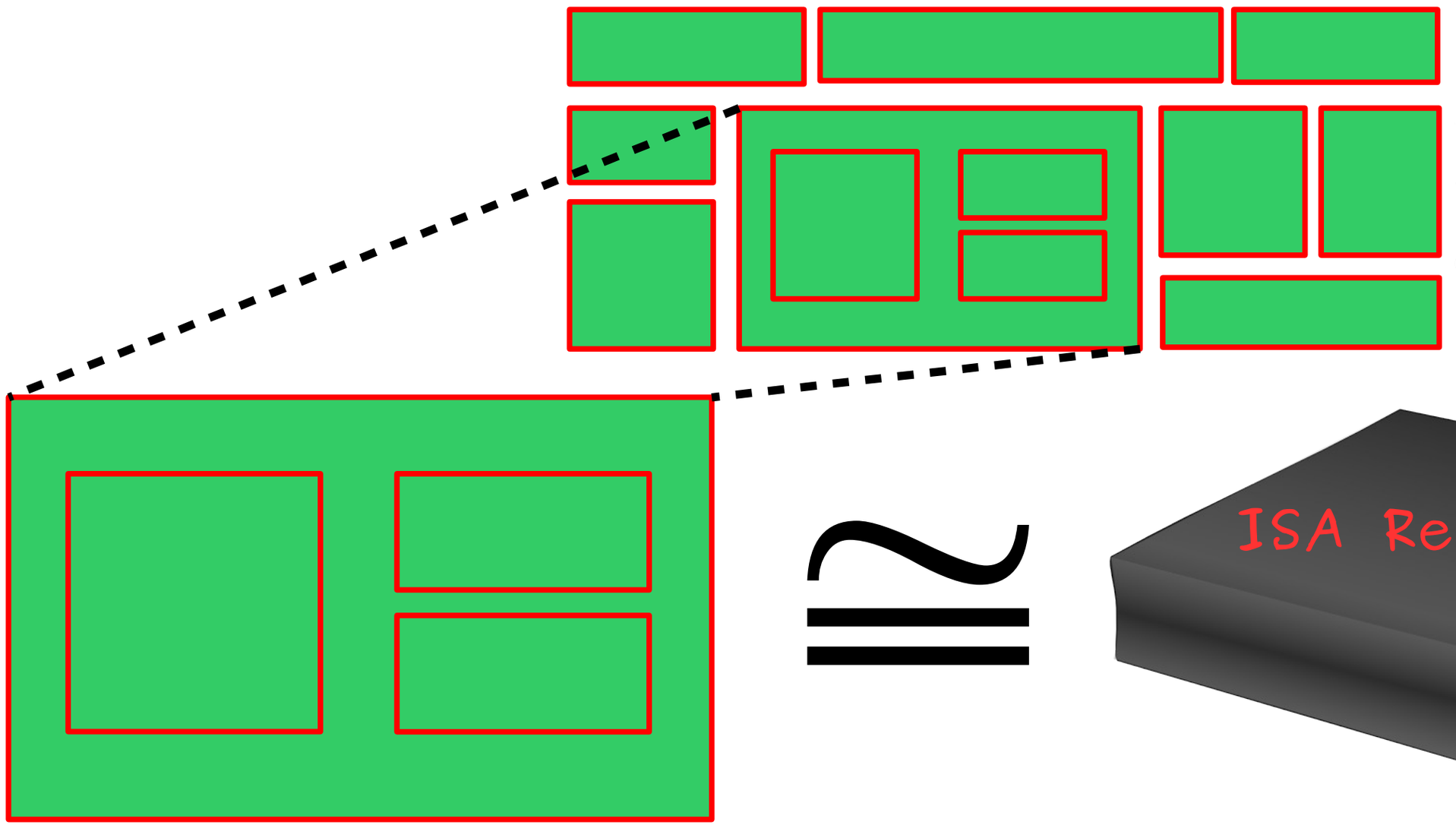
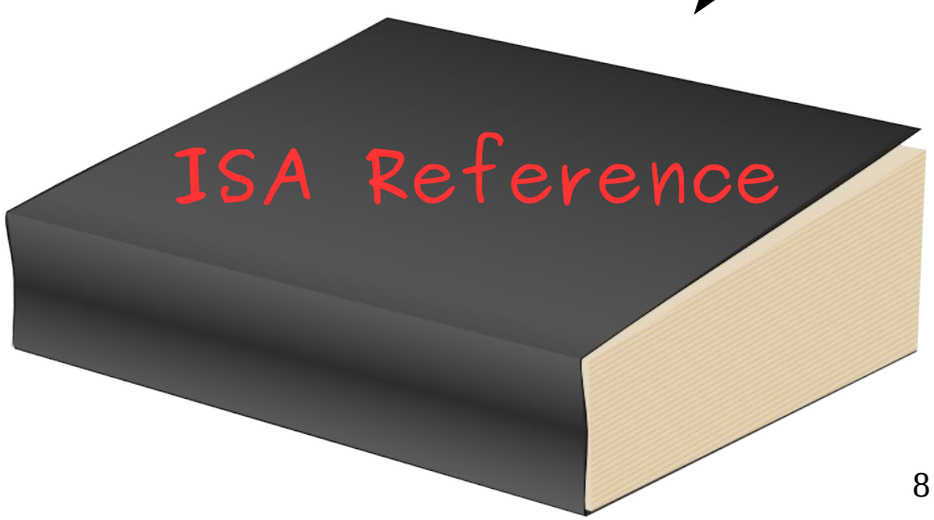


The Kami way:
Behavioral refinement
of functional spec



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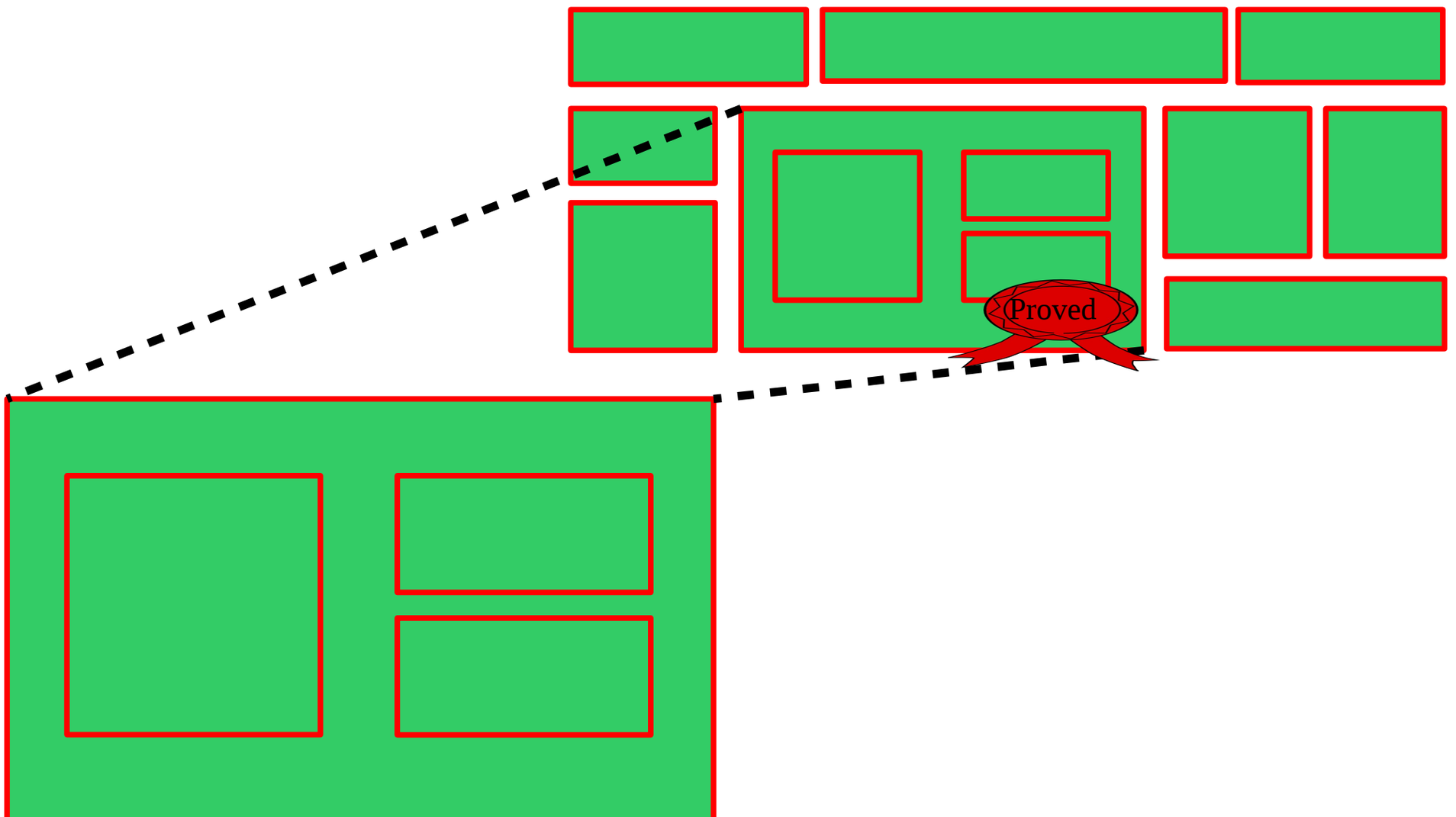

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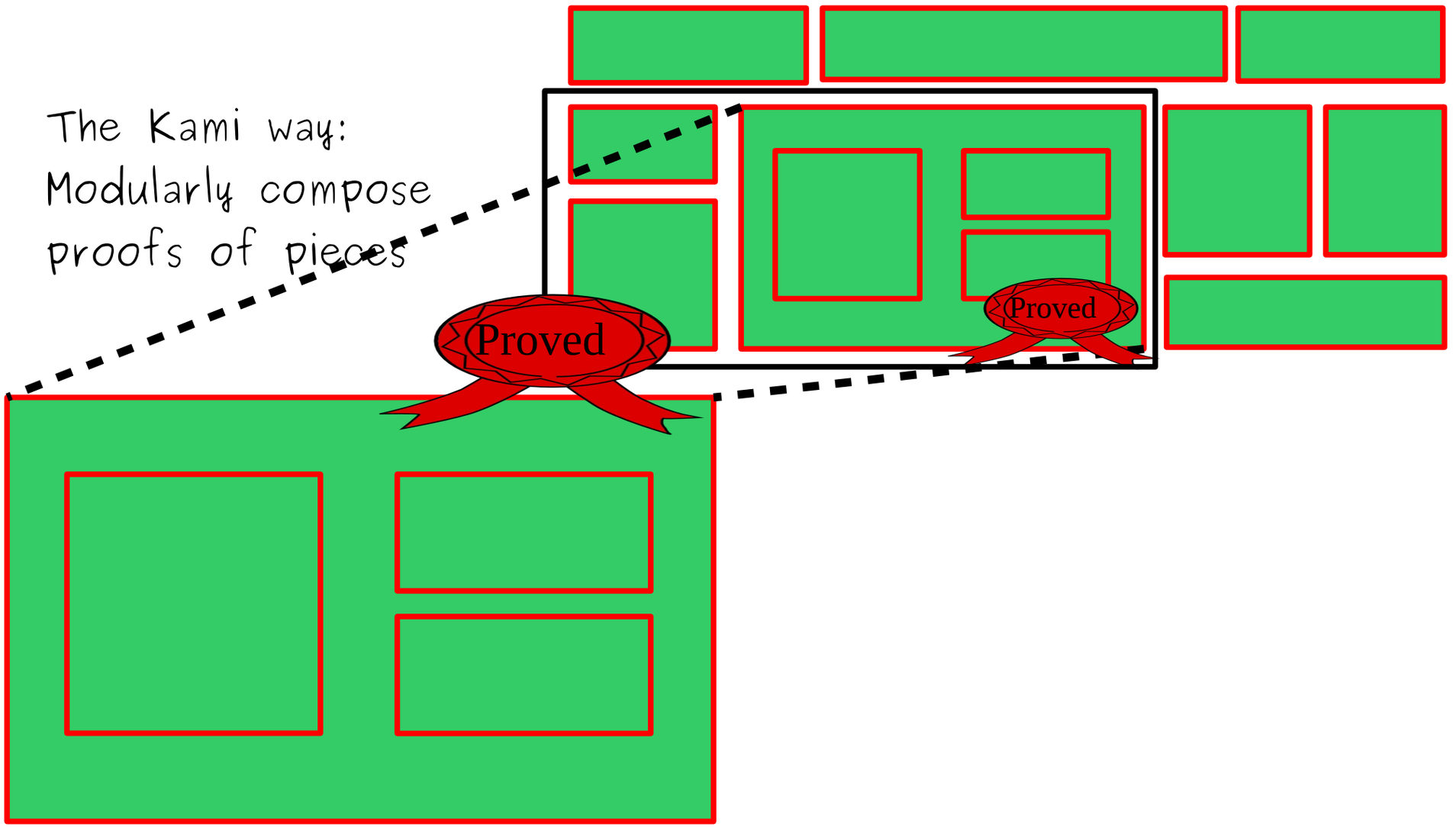
Modularly compose
proofs of pieces



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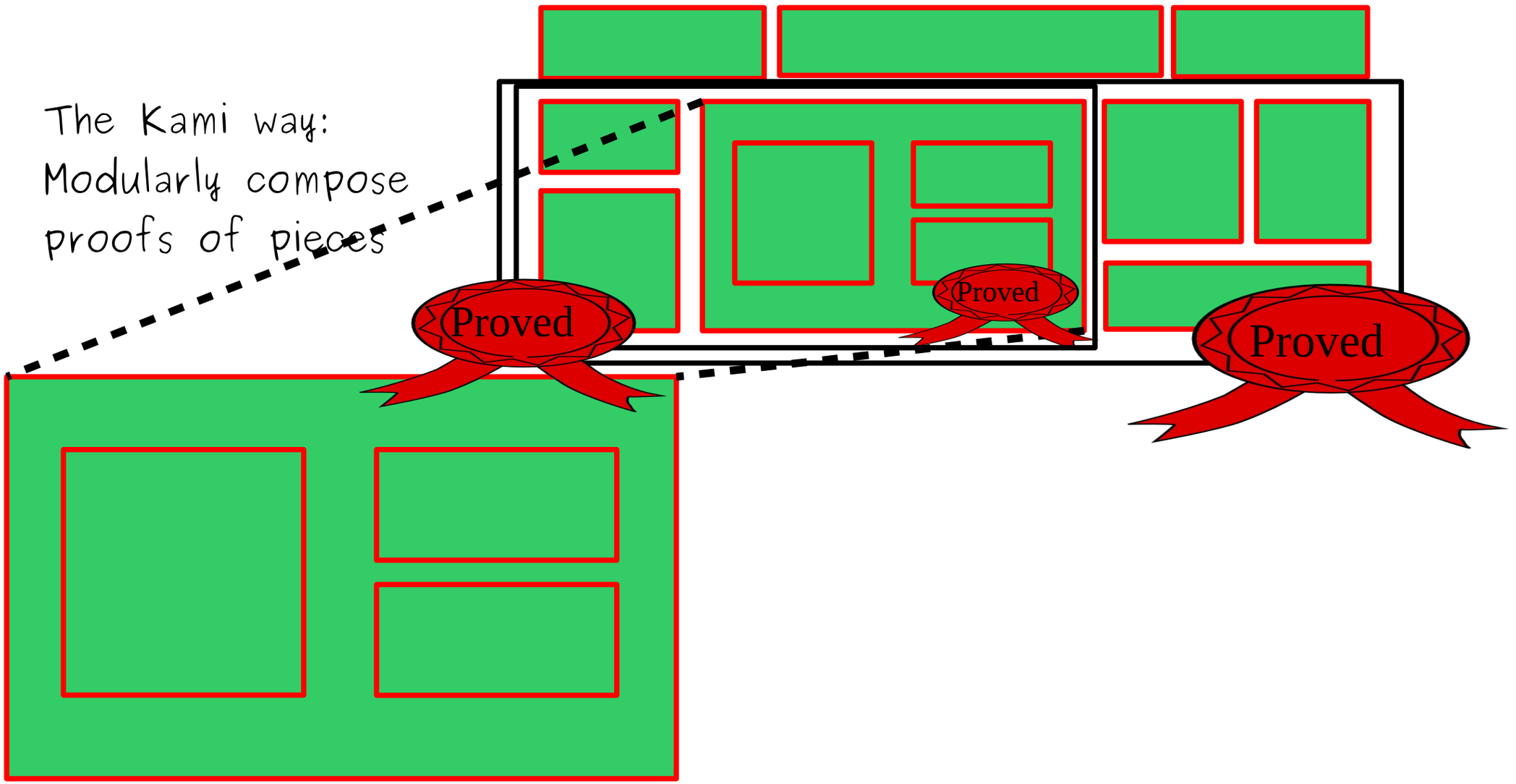

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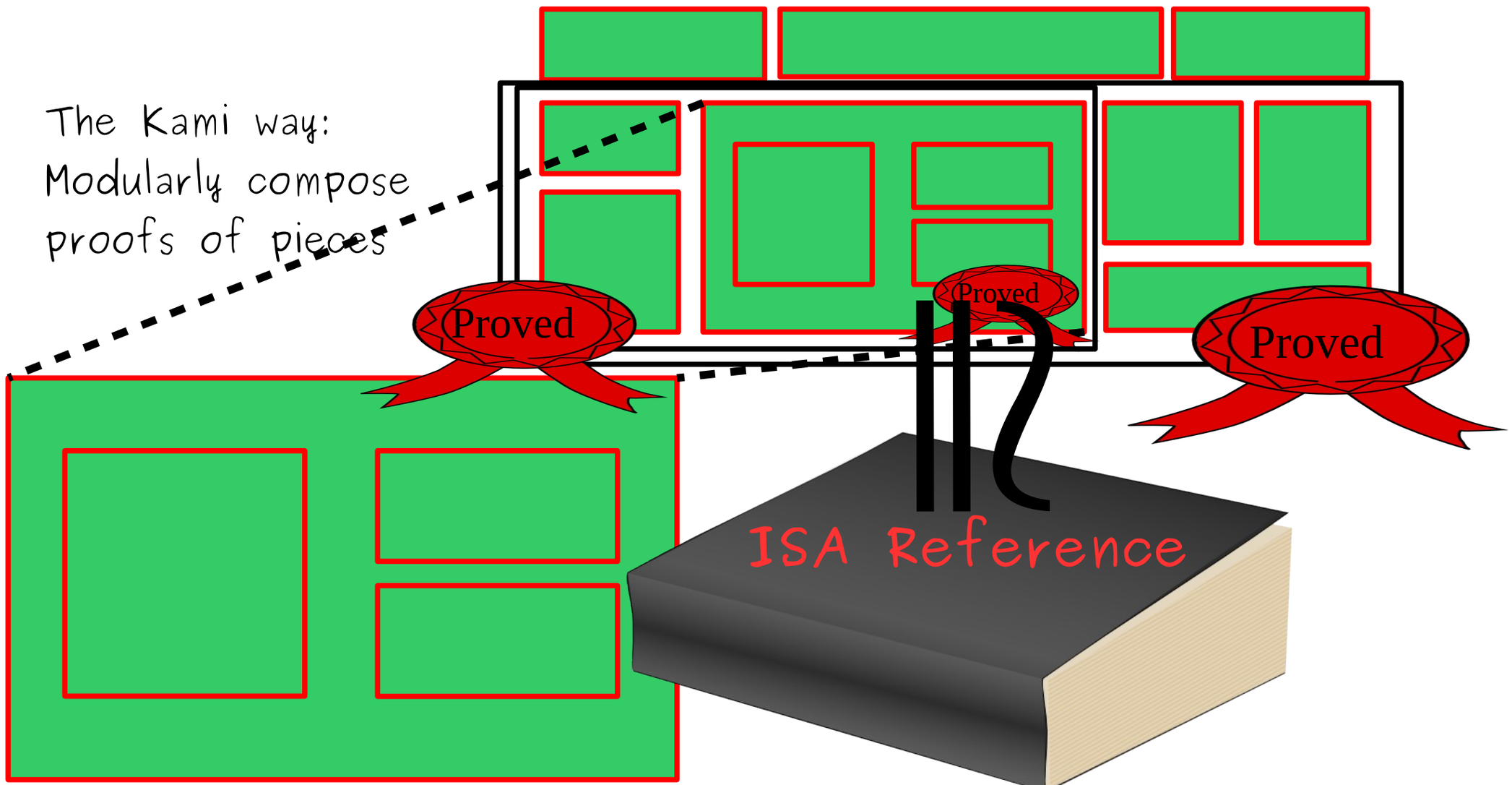

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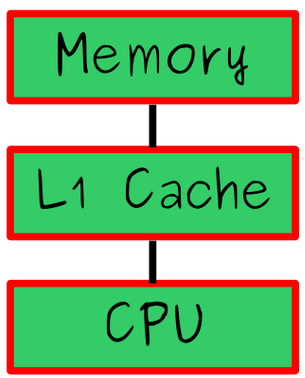

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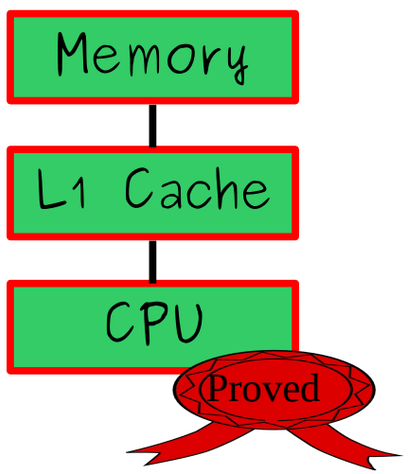

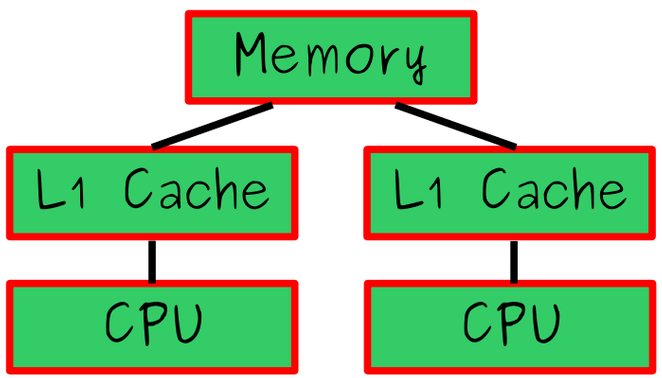

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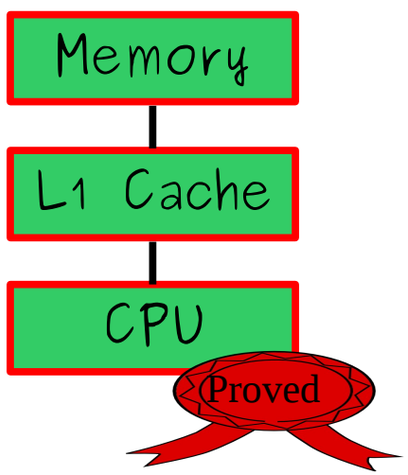

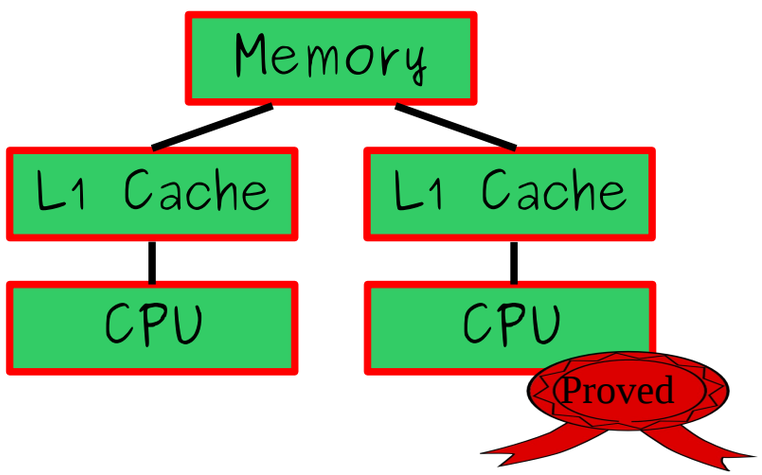

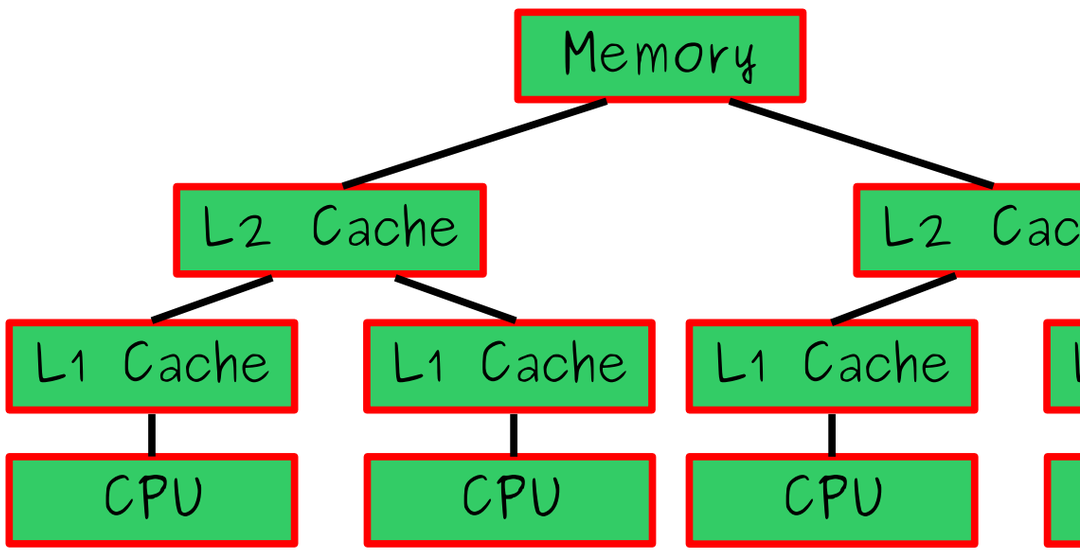

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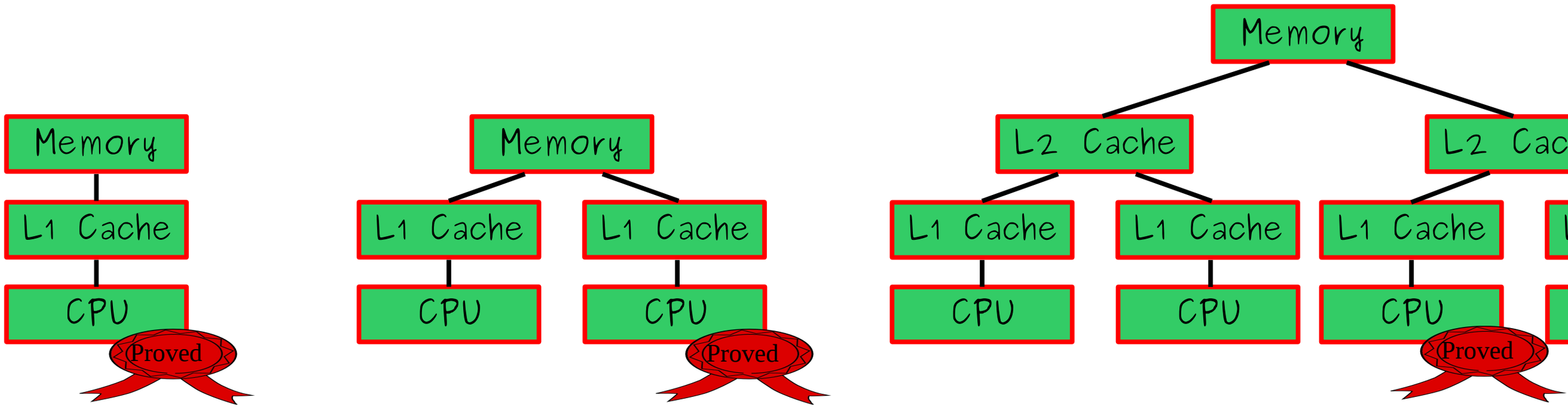

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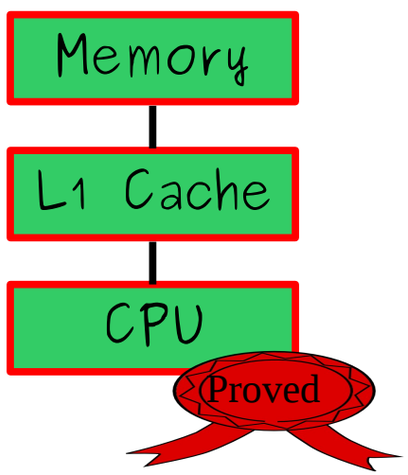
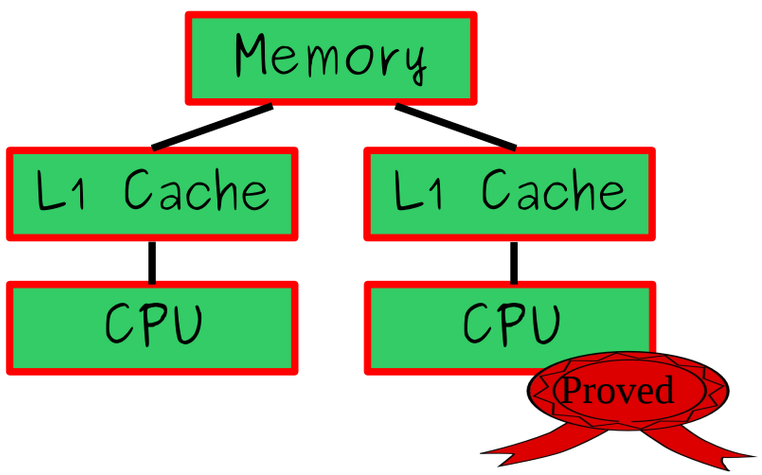
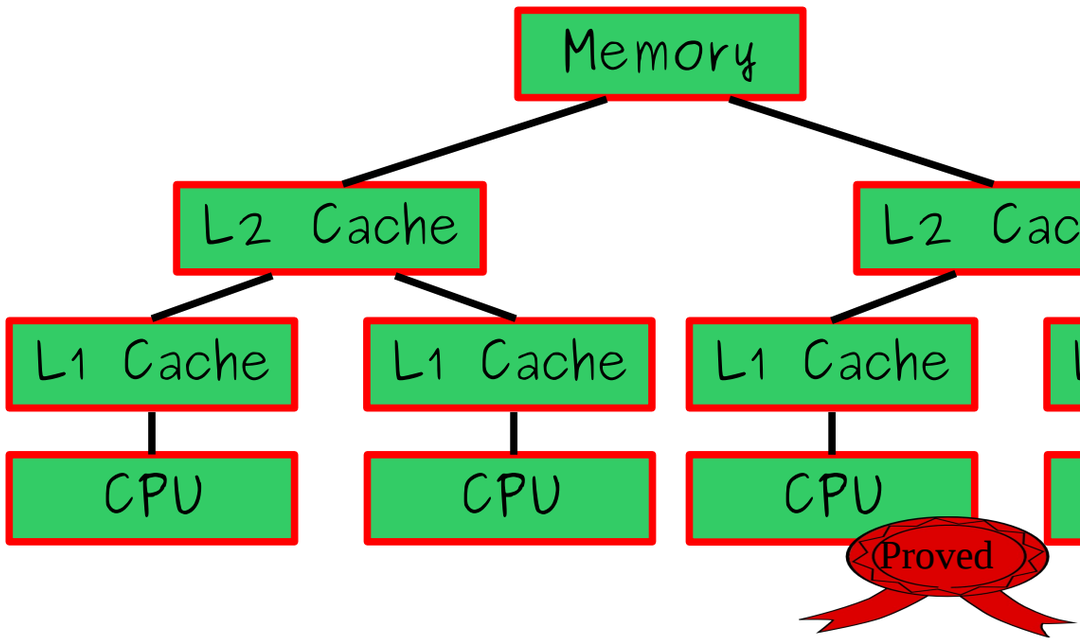
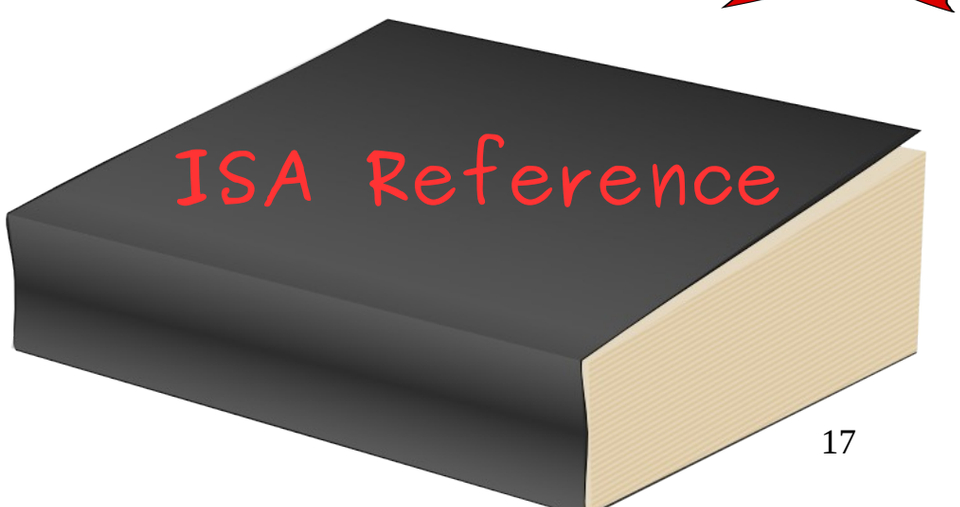






The Kami way:
Prove once for all parameters

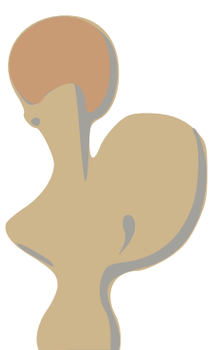
∀ trees. ≅



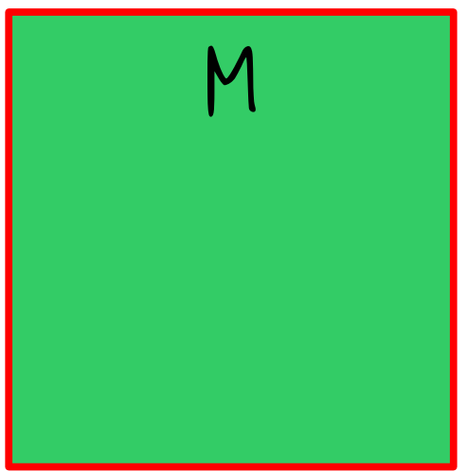
A **framework** to support *implementing, specifying, formally verifying,* and *compiling* hardware designs

based on the **Bluespec** high-level hardware design language

and the **Coq** proof assistant



The Big Ideas (from Bluespec)



Program modules are objects

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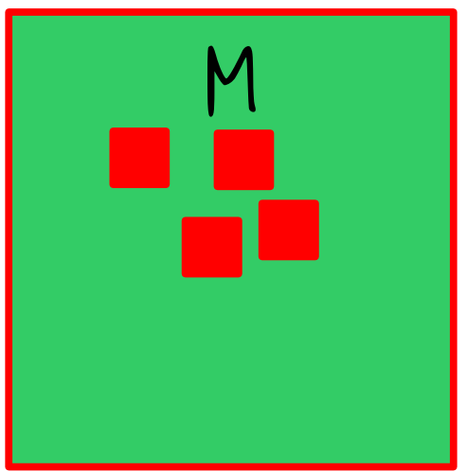

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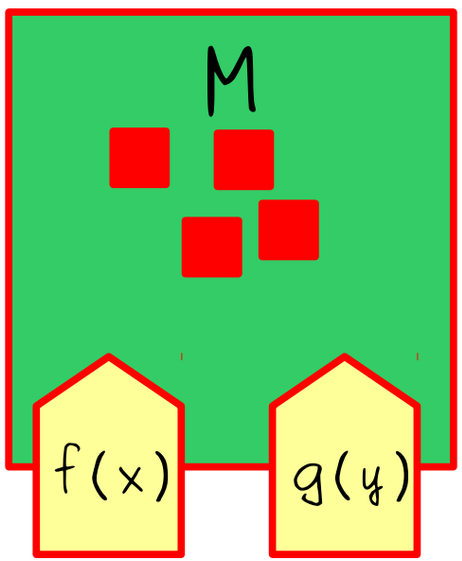

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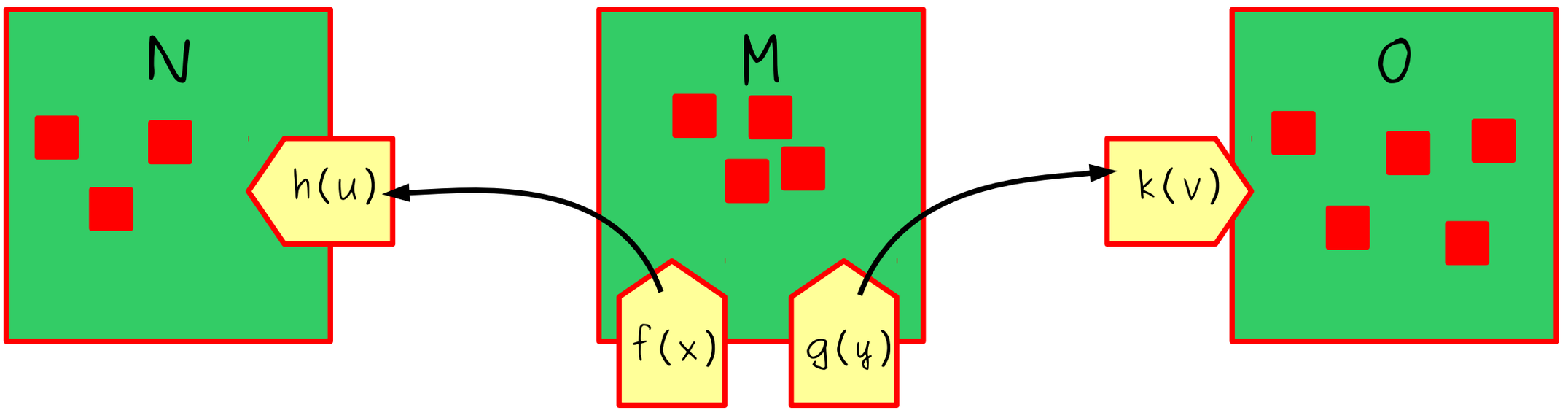

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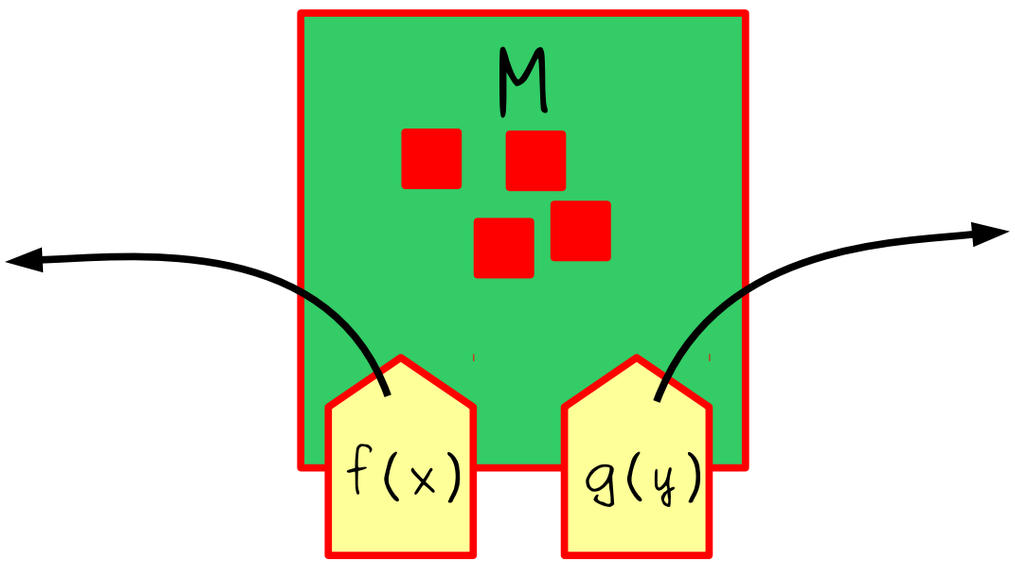

Every method call appears to execute **atomically.**

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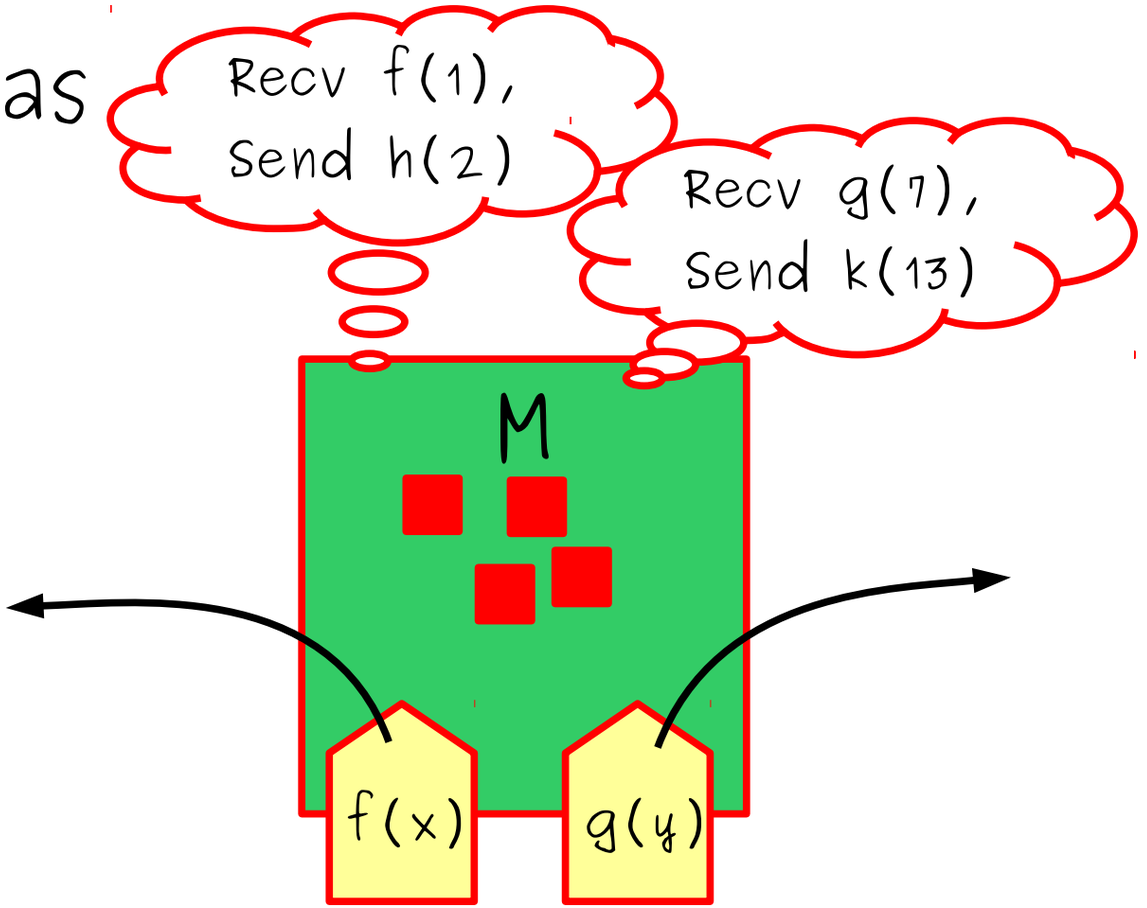

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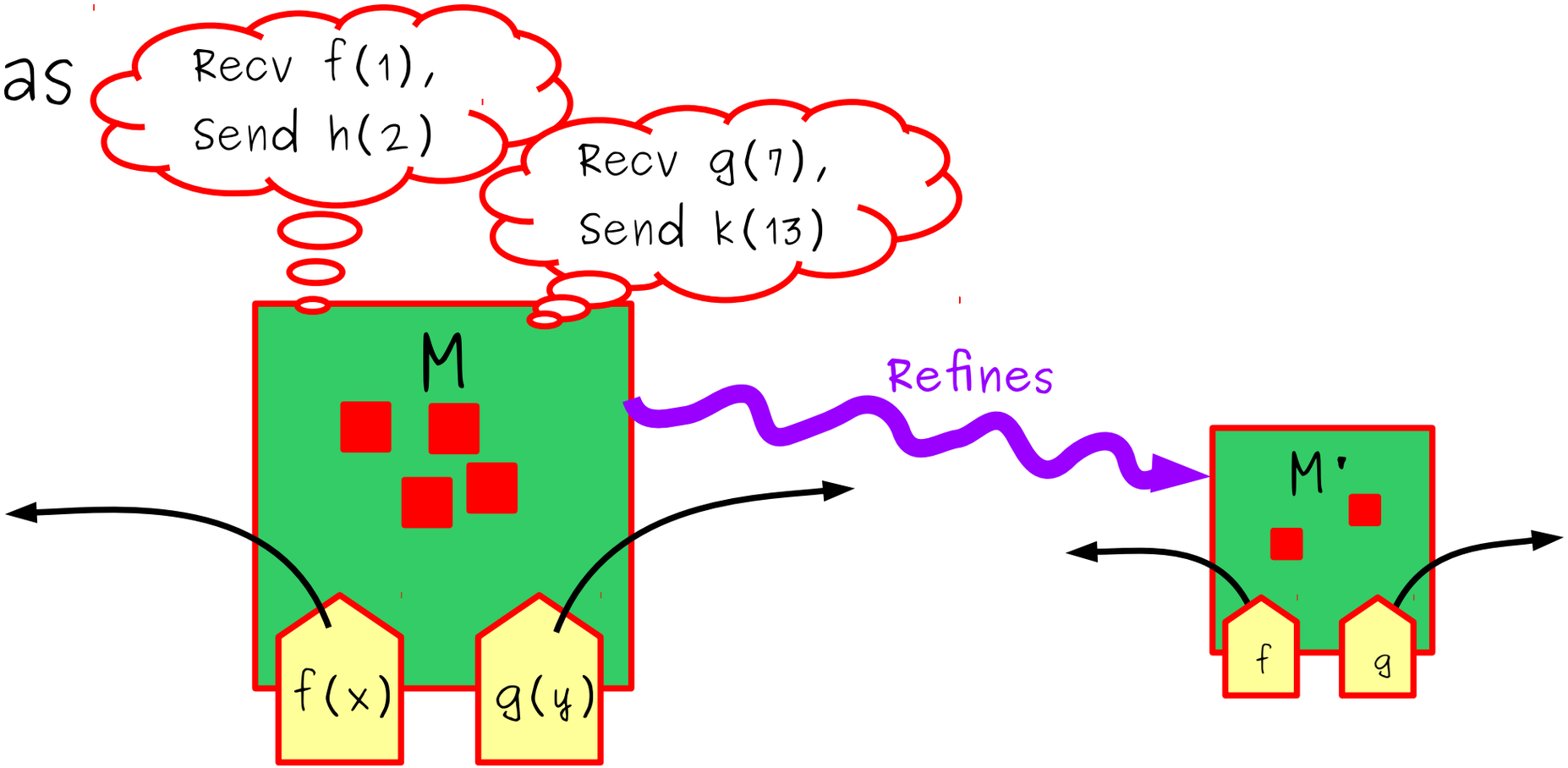

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Object *refinement* is inclusion of possible traces.

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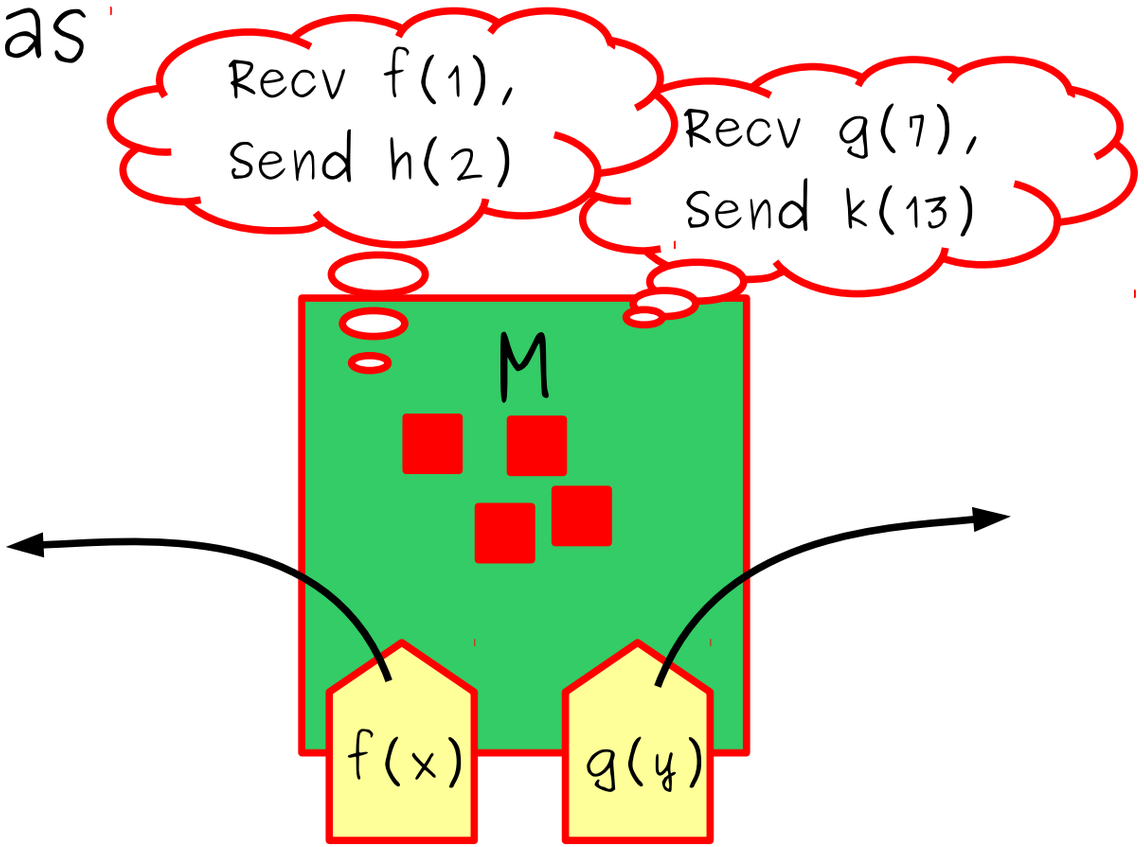

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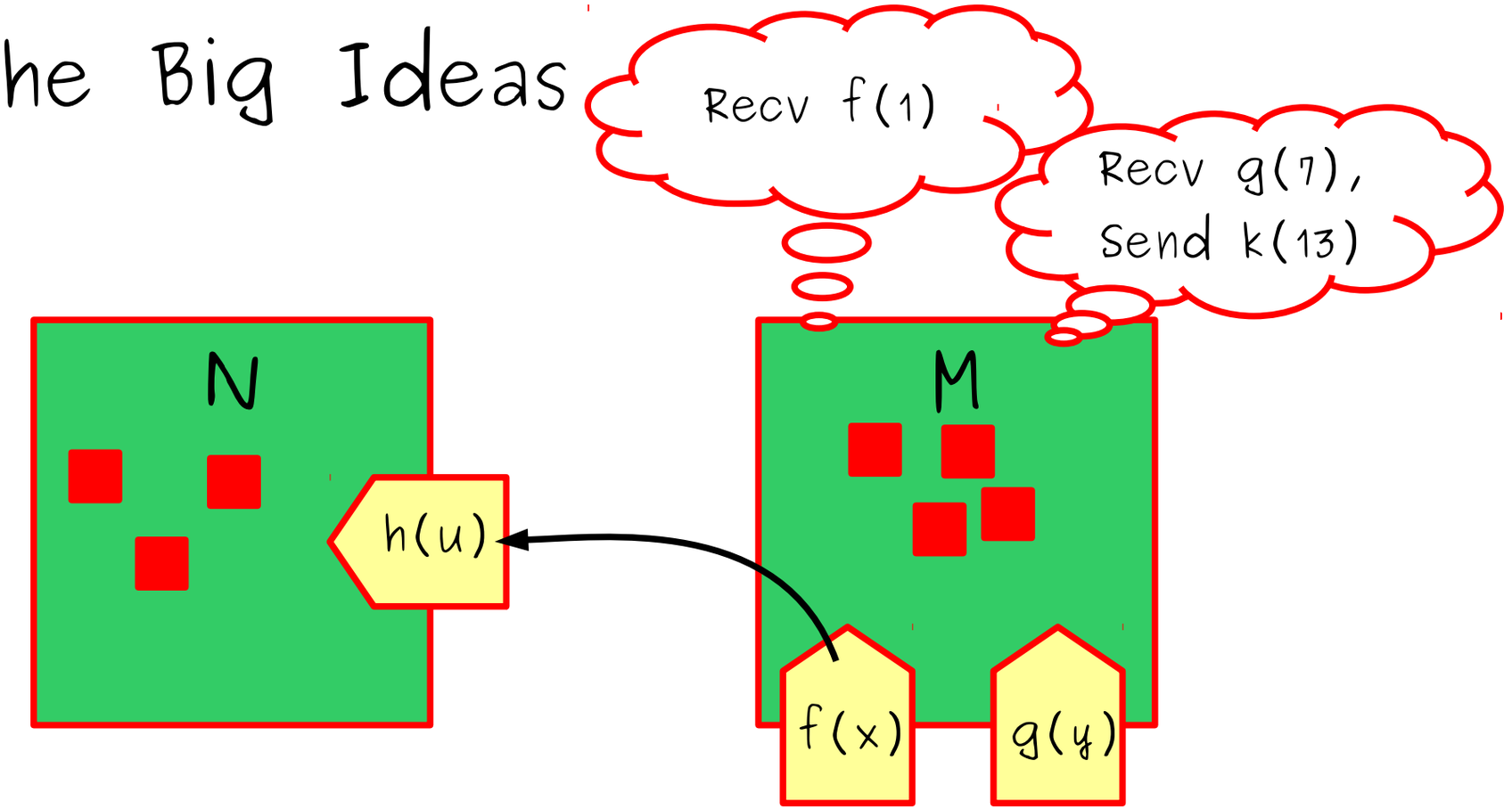

Composing objects hides internal method calls.

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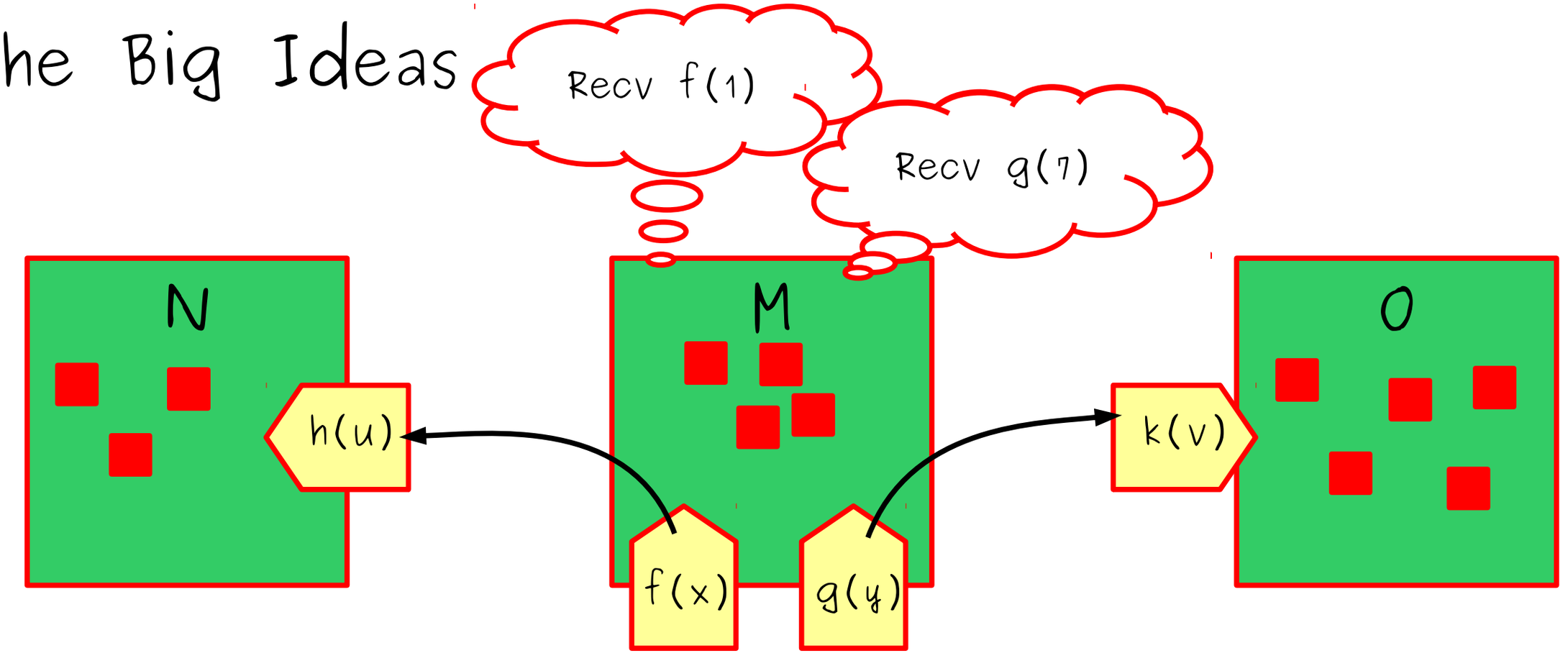

Composing objects hides internal method calls.

Some Example Kami Code (simple FIFO)

```
Definition deq {ty} : ActionT ty dType :=
  Read isEmpty <- ^empty;
  Assert !#isEmpty;
  Read eltT <- ^elt;
  Read enqPT <- ^enqP;
  Read deqPT <- ^deqP;
  Write ^full <- $$false;
  LET next_deqP <- (#deqPT + $1) :: Bit sz;
  Write ^empty <- (#enqPT == #next_deqP);
  Write ^deqP <- #next_deqP;
  Ret #eltT@[#deqPT].
```

An Example Kami Proof (pipelined processor)

```
Lemma p4st_refines_p3st: p4st <<== p3st.
Proof.
  kmodular.
  - kdisj_edms_cms_ex 0.
  - kdisj_ecms_dms_ex 0.
  - apply fetchDecode_refines_fetchNDecode; auto.
  - krefl.
Qed.
```

Uses standard **Coq** ASCII syntax for mathematical proofs.

These proofs are checked **automatically**, just like type checking.

We inherit streamlined **IDE support** for Coq.

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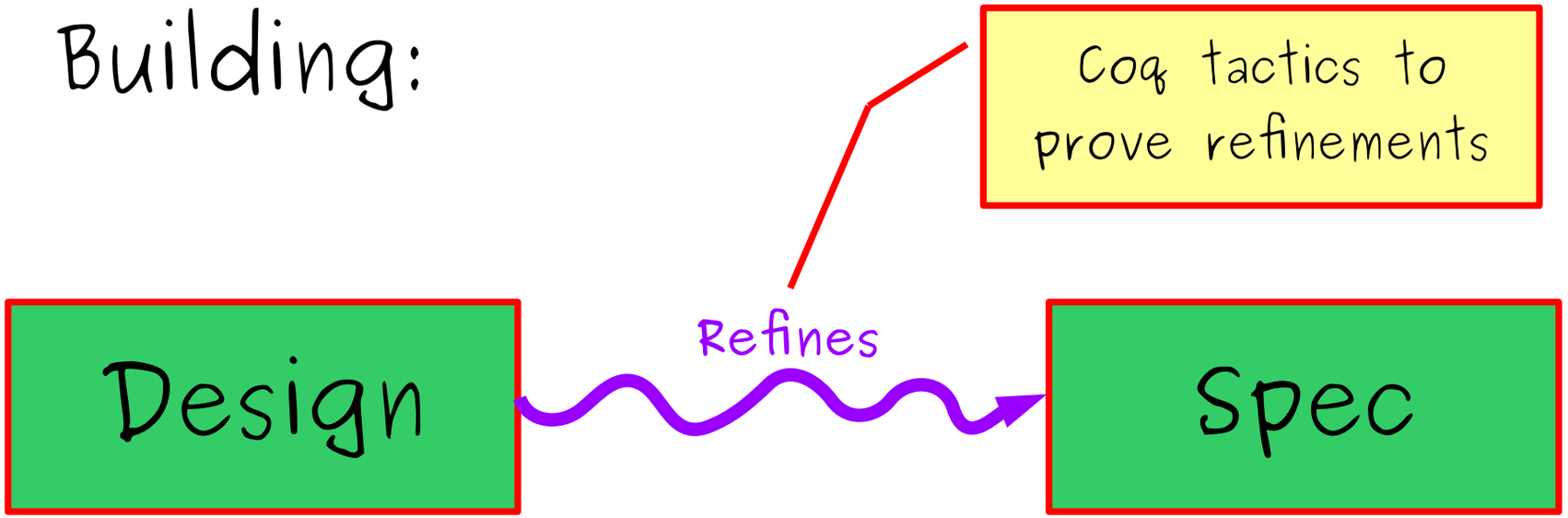

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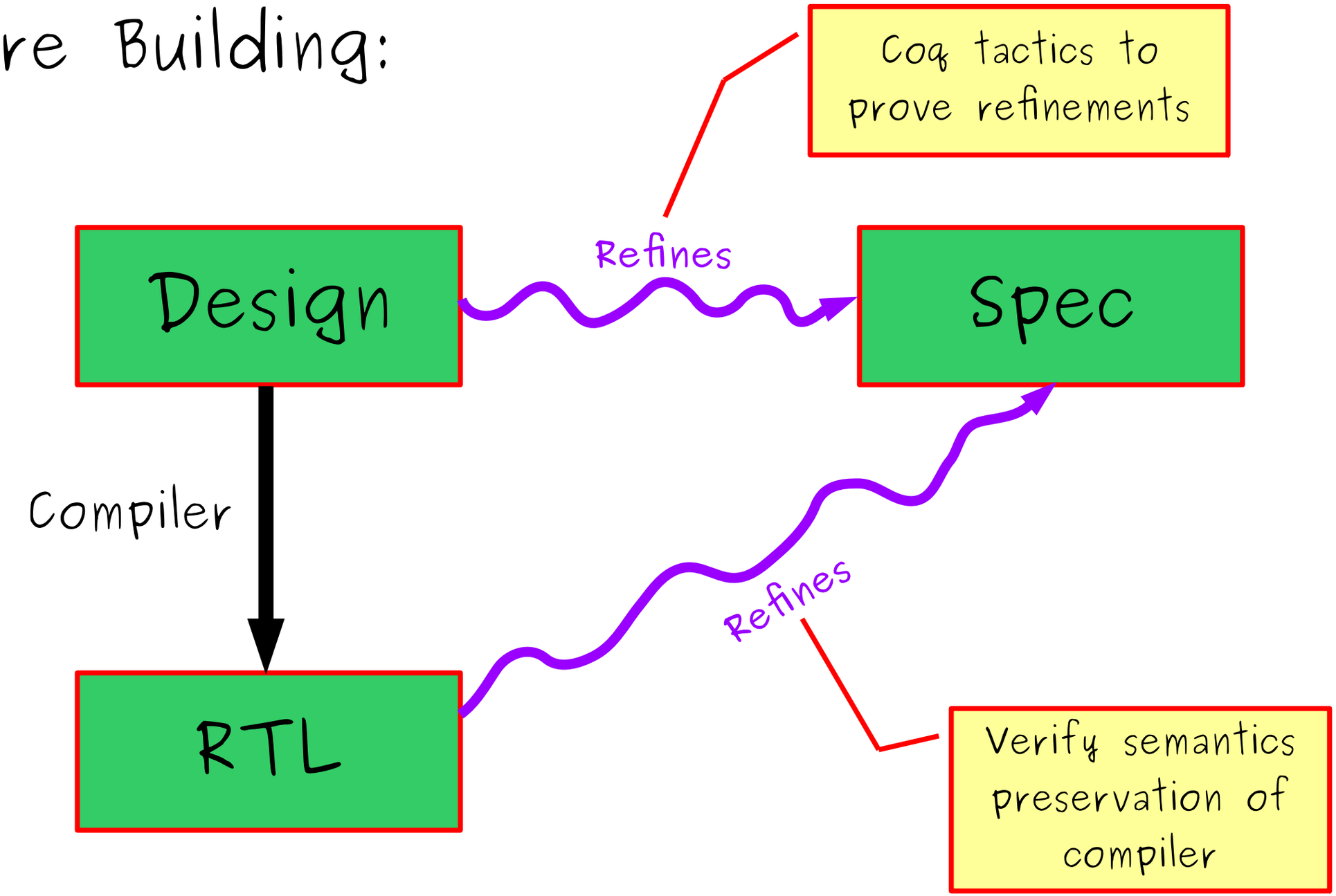
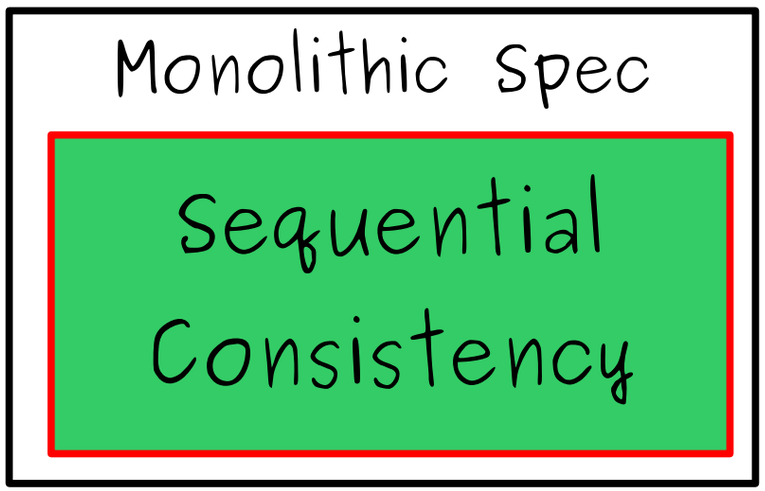


Some Useful Refinement Tactics



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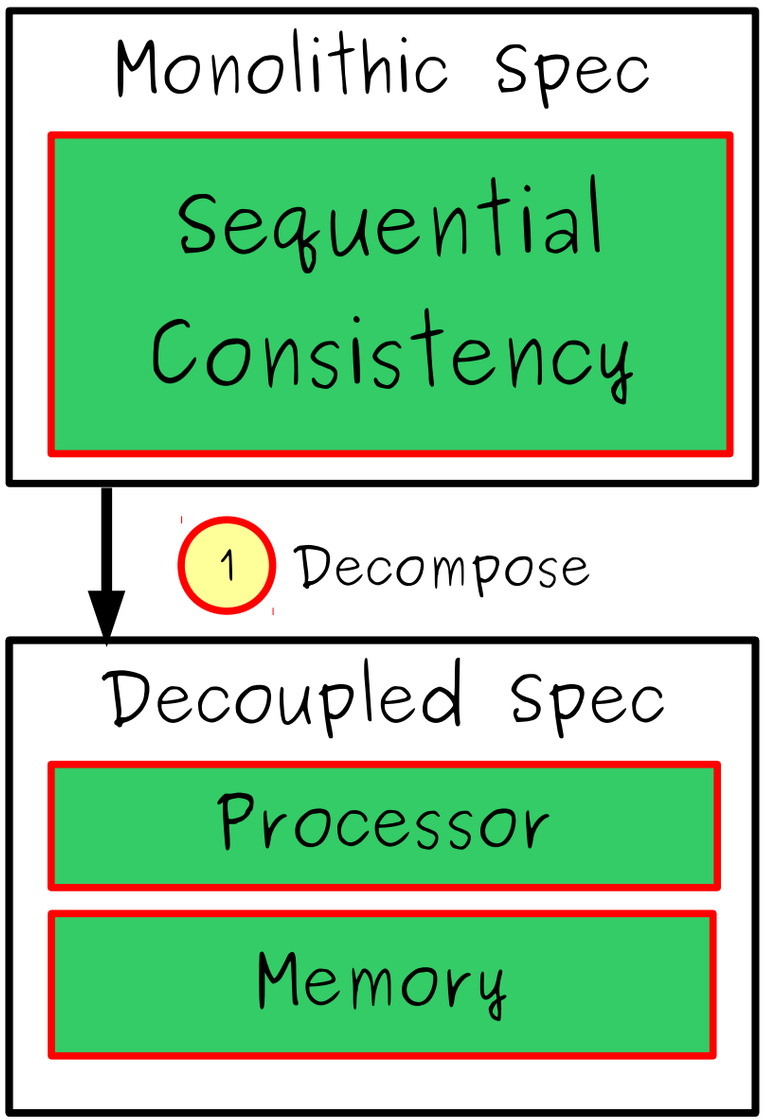

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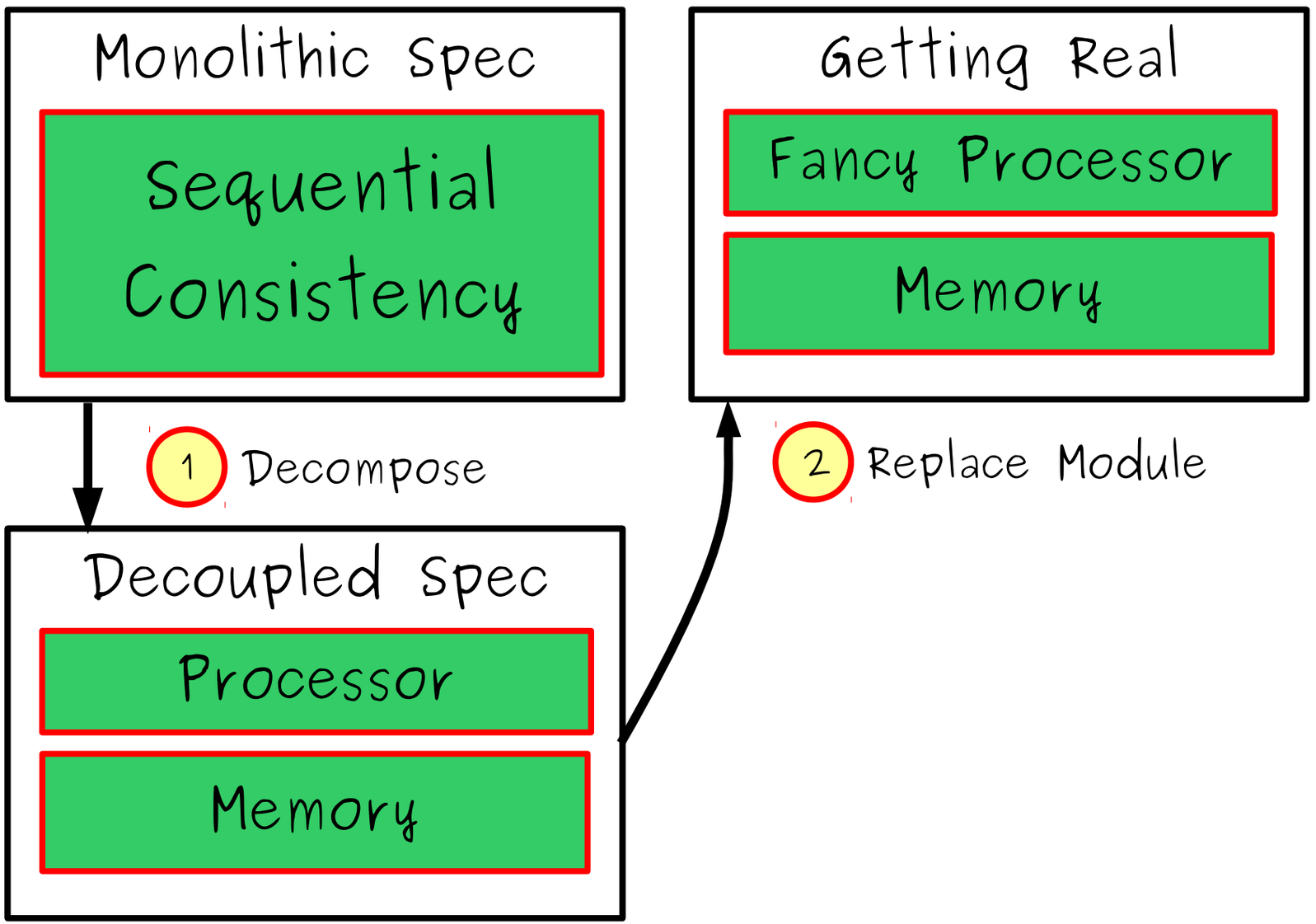

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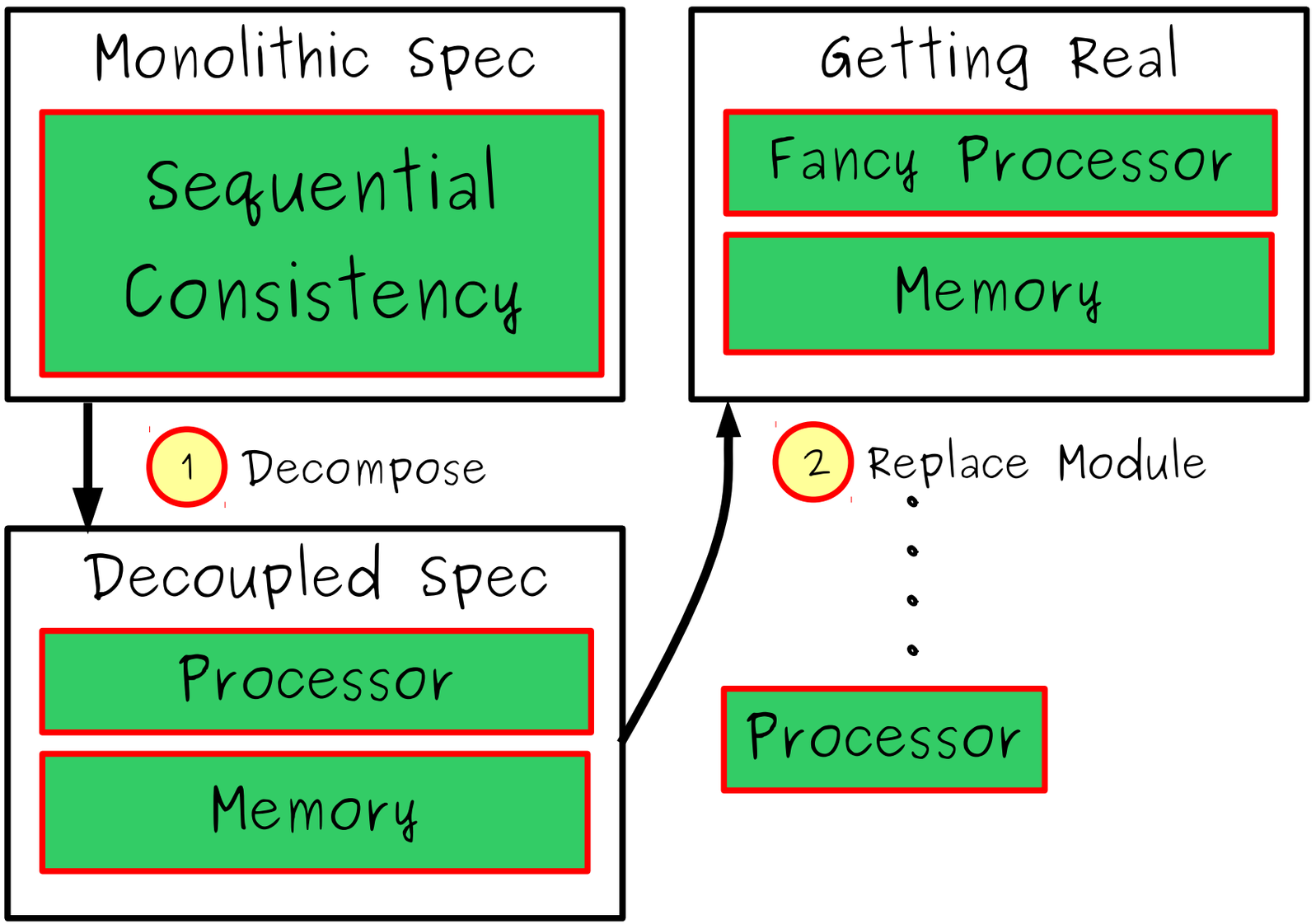

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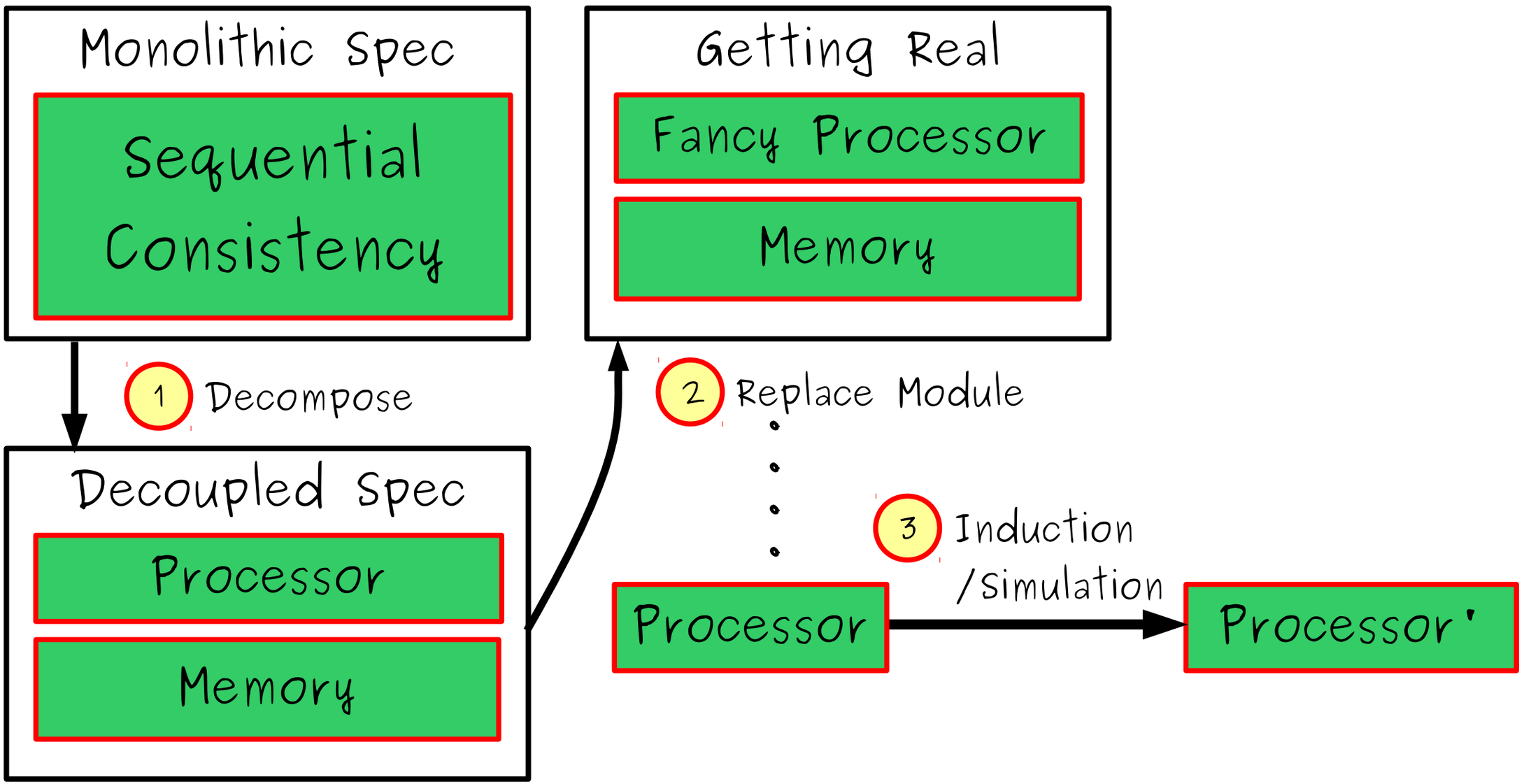

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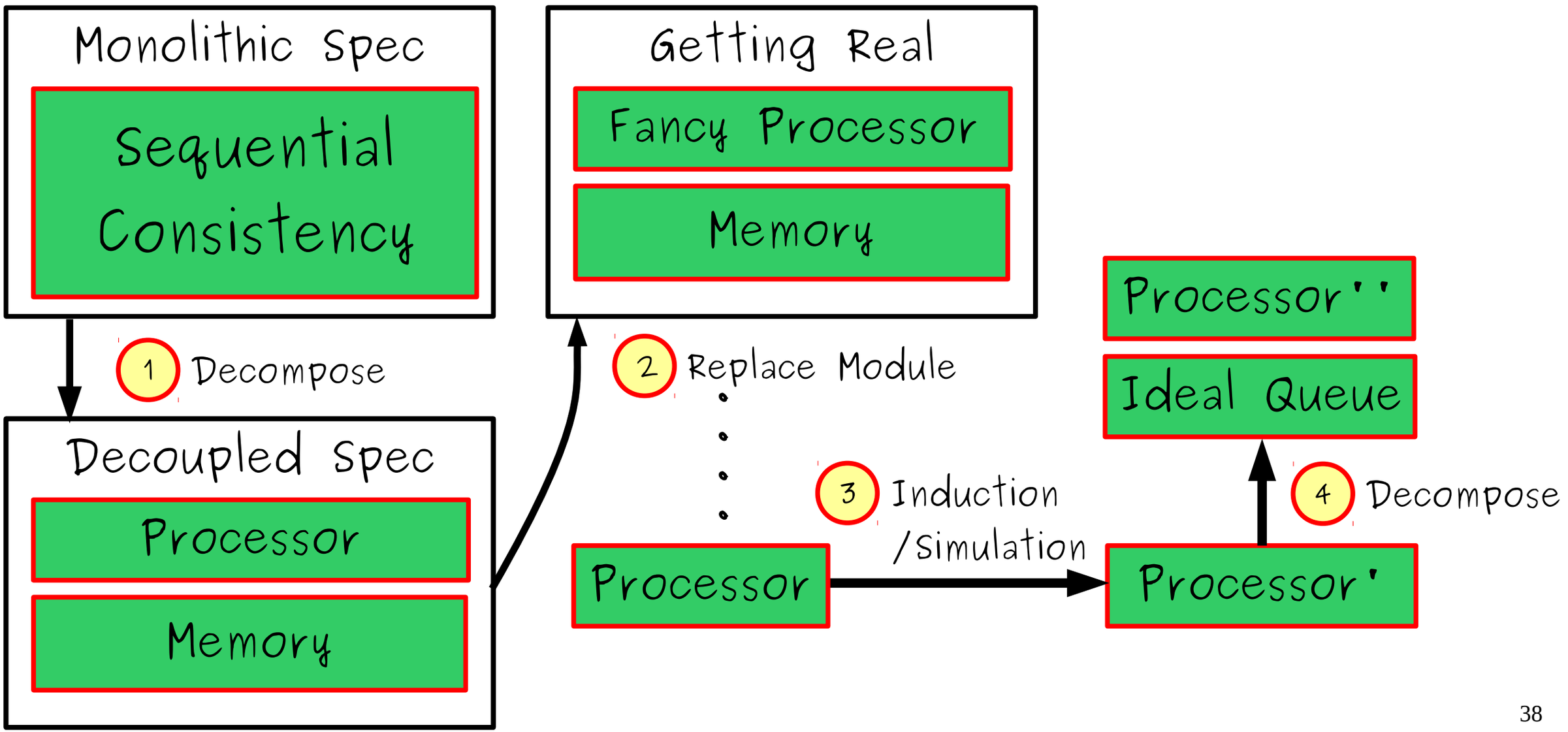

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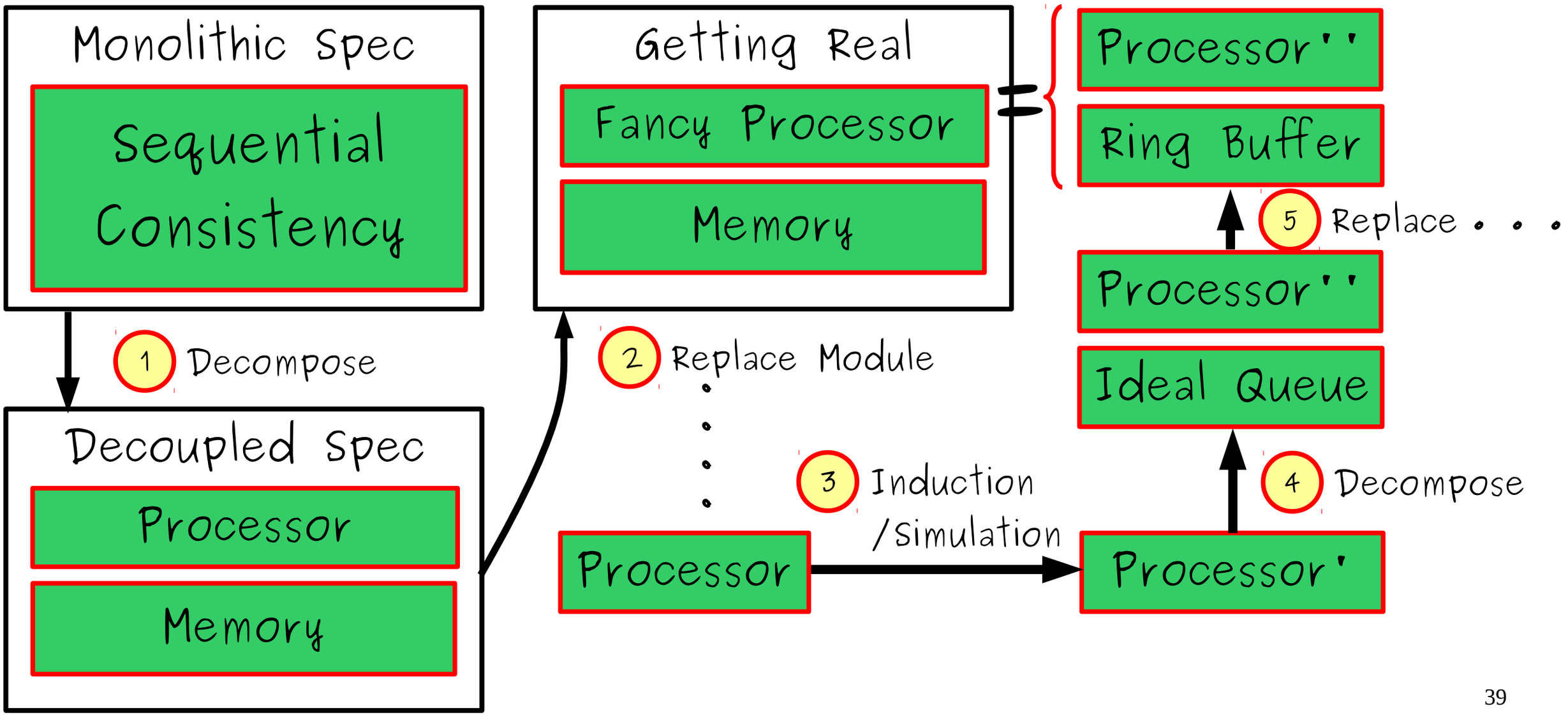


Key Ingredient

Formal Semantics for RISC-V ISA(s)

Nikhil just explained the semantics style.
We are building a translator for the semantics into the language of Coq/Kami.

An Open Library of Formally Verified Components

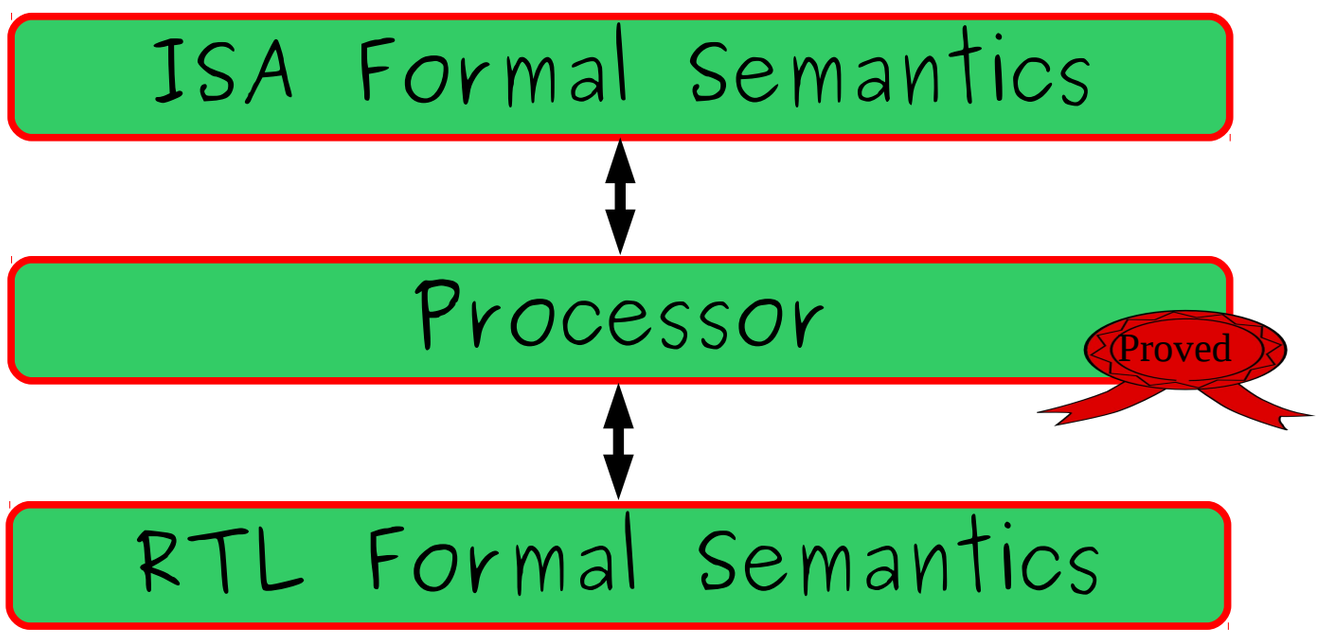
- Microcontroller-class RV32I (multicore; U)
- Desktop-class RV64IMA (multicore; U,S,M)
- Cache-coherent memory system

Reuse our proofs when composing our components with your own formally verified **accelerators**!

The Promise of this Approach

ISA Formal Semantics

The Promise of this Approach



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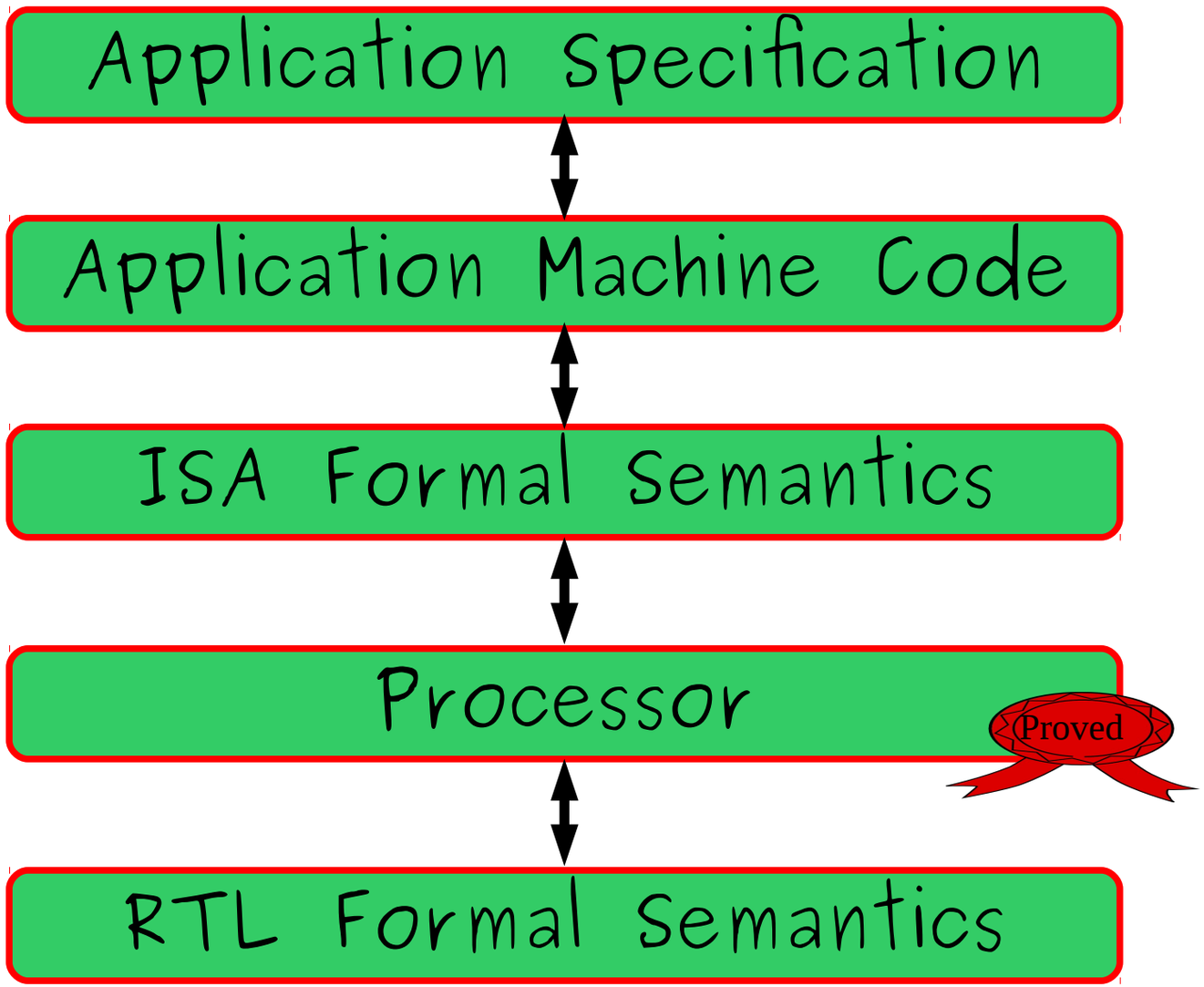

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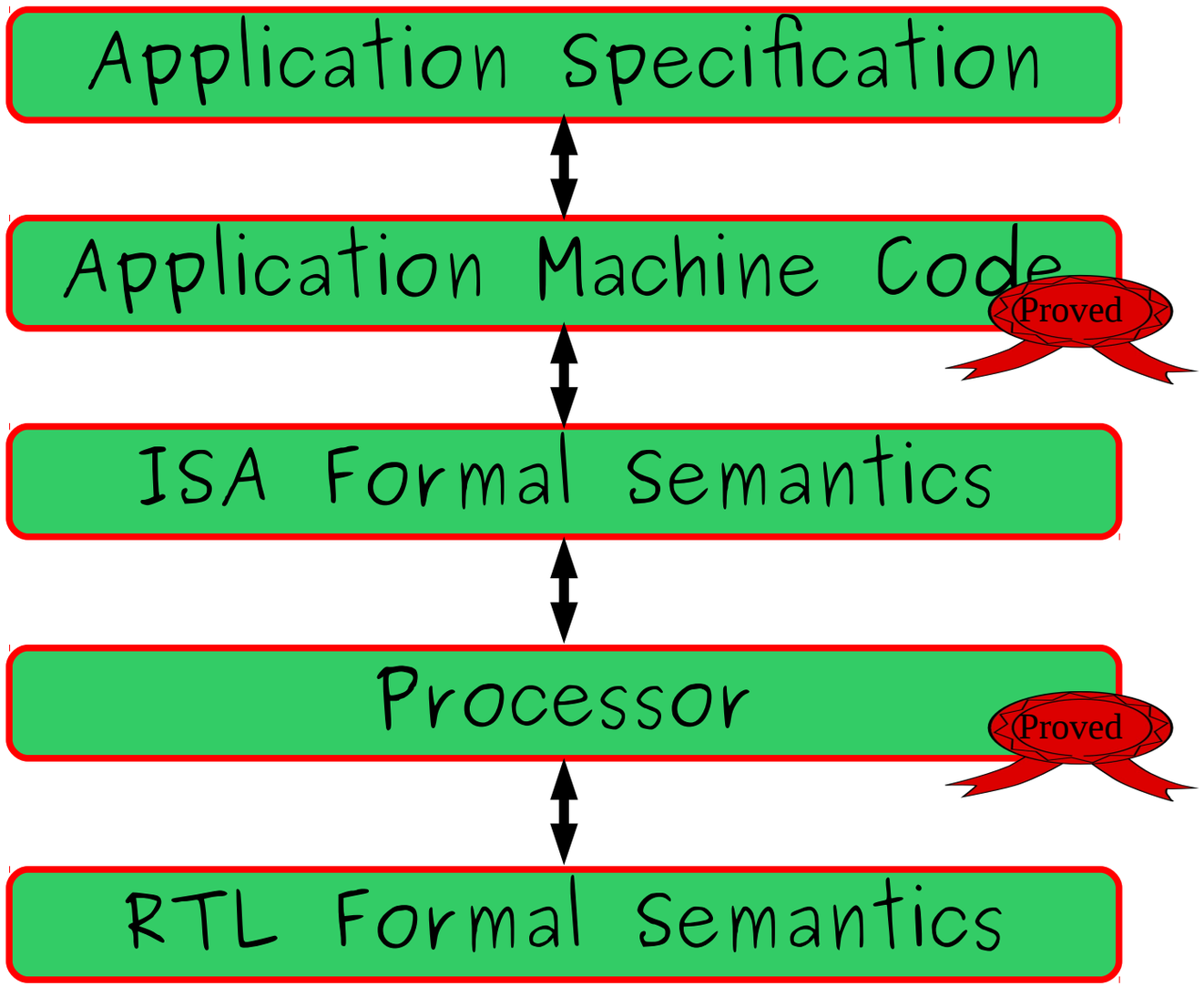

The Trusted Computing Base

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- ☑ Coq proof checker (small & general-purpose)
- ☑ RTL formal semantics
- ☑ Application specification

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- [x] Coq proof checker (small & general-purpose)
- [x] RTL formal semantics
- [x] Application specification
- [ ] ISA formal semantics
- [ ] Hardware design (Bluespec, RTL, …)
- [ ] Software implementation (C, …)

Shameless plug:

Part of a larger project:
The Science of Deep Specification
A National Science Foundation
Expedition in Computing

https://deepspec.org/

Join our mailing list for updates on our 2018 summer school: hands-on training with these tools!