RISC5: Improving Support for RISC-V in gem5

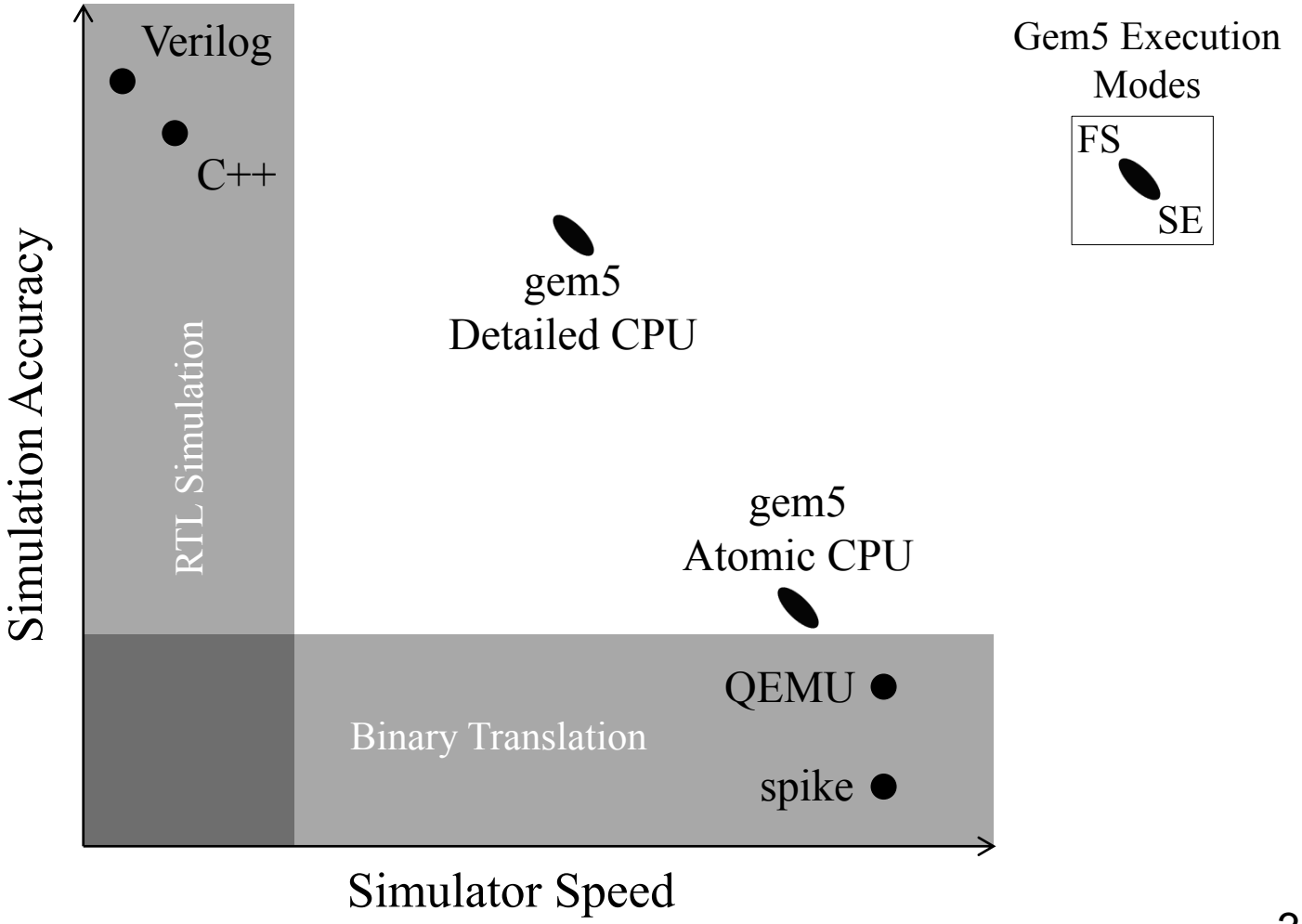
Alec Roelke (ar4jc@virginia.edu)
Mircea R. Stan (mircea@virginia.edu)

Introduction

- Increasing complexities of designs increases simulation overhead
- Proprietary libraries and architectures impede research and collaboration
- Solution: gem5—fast, flexible, free
- Useful for RISC-V hardware development

N. Binkert *et al.*, *SIGARCH* vol. 39 no. 2, 2011

RISC-V Simulation Platforms



A. Roelke and M. Stan, *CARRV* 2017

Implementation of RISC-V in gem5

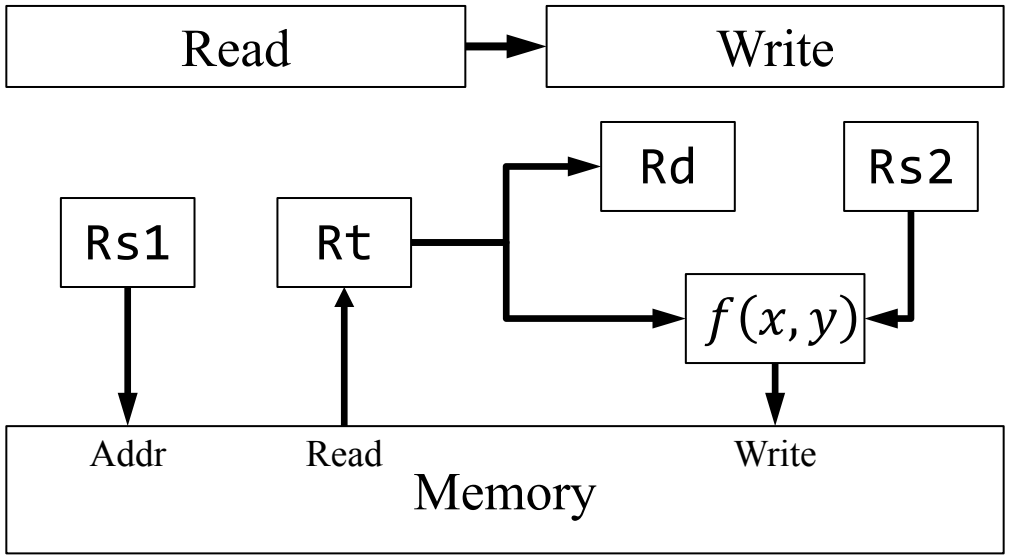
- Includes 64-bit base ISA + standard, compressed extensions (RV64GC)
- Supports single-threaded execution in SE mode
- No support for privileged ISA yet

Integer and Multiply Instructions

- Most instructions based on MIPS
  - e.g. `fence` (RISC-V) : `sync` (MIPS)
- Internal behaviors mostly copied from MIPS and Alpha
- Nearly all instructions implemented
  - Only `eret` has no implementation
  - `fence` does not support ordering flags

Atomic Instructions

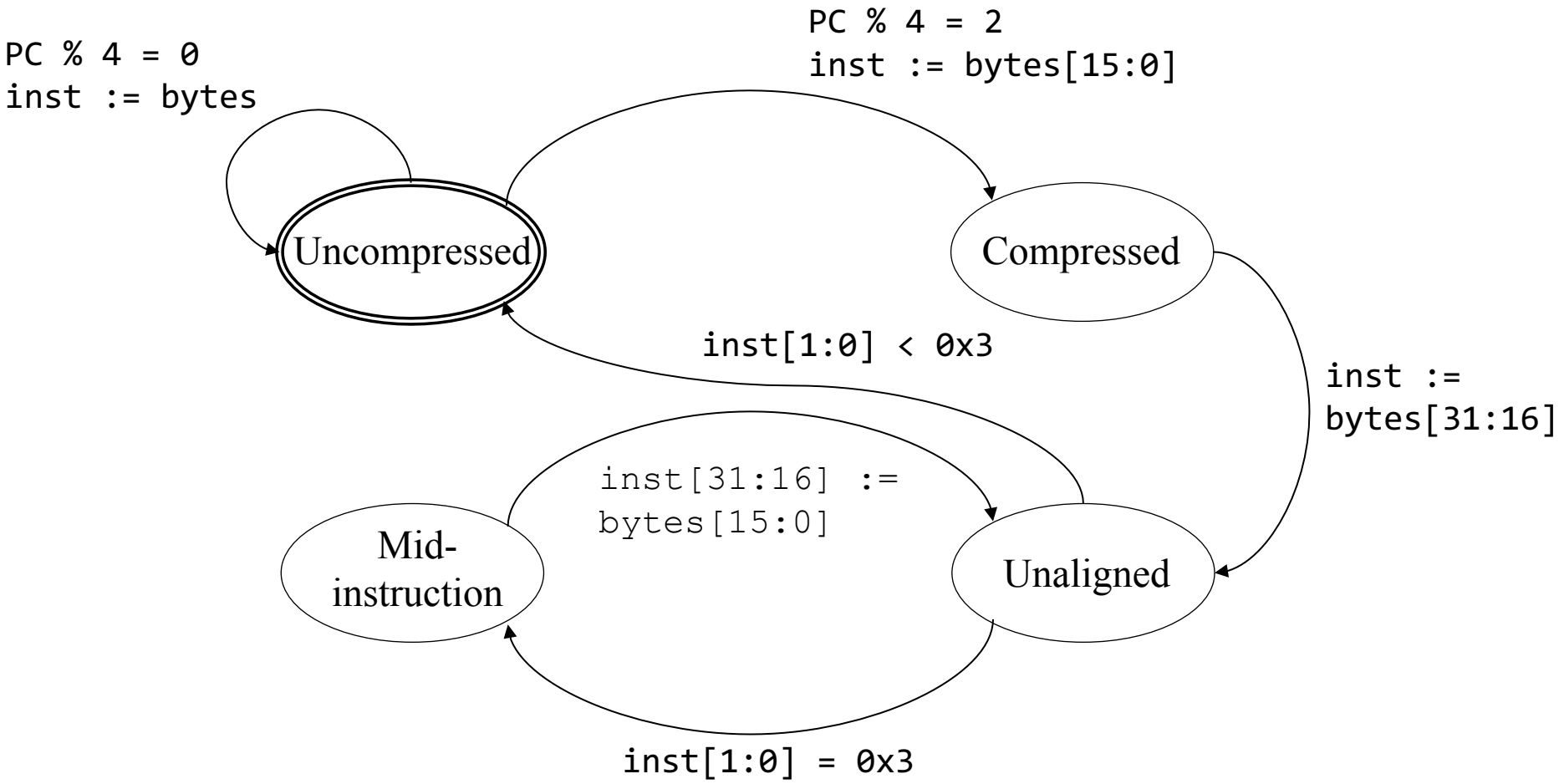
- *Release Consistency*: acquire an address to see changes after earlier release
- LR/SC and atomic RMW
- Mark with `ACQUIRE` or `RELEASE`



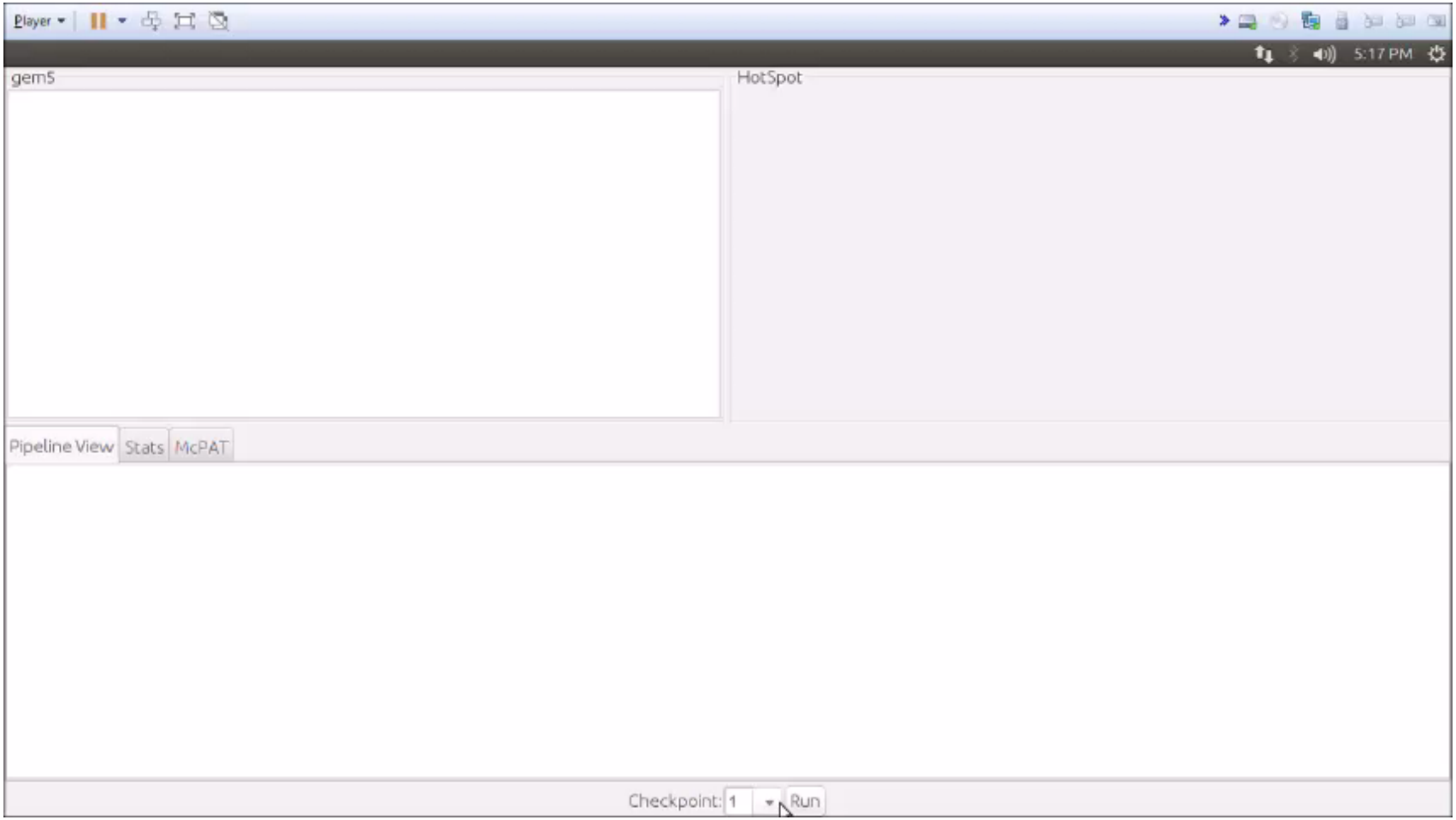
Floating-Point Instructions

- Development machine missing max magnitude round mode
- Verified against spike and a hardware design
  - Invalid computation results (NaN, ∞, 0)
  - Floating point exceptions

Compressed Instructions



Using RISC5 in a Tool Flow



hplp

Future Work

- Multithreaded workloads in SE mode
  - m5threads to support RISC-V
  - Gem5 to support pthreads
- Full-system mode
  - Requires privileged ISA
- Correct minor differences
  - e.g. floating-point rounding

Conclusion

- Implemented RISC-V in gem5
- Significant work left until full support
- RISC5 is available as part of the main gem5 release at www.gem5.org
- Acknowledgments:
  - Pradip Bose, Schuyler Eldridge, and the rest of the IBM VELOUR Team
  - Members of the HPLP research group
  - The gem5 community