Western Digital®

RISC-V ISA: Understanding Limitations and Methods to improve code density & performance

Western Digital & RISC-V

RISC-V

NEWS

eeNews Embedded Interview With Martin Fink, CTO Of Western Digital At The RISC-V Workshop

DATE: MAY 11, 2018

Western Digital 'stores' almost half of the world's data. For the new generation of data memory products, Western Digital, Platinum Member of the RISC-V Foundation, started researching and developing with the RISC-V Instruction Set Architecture. Martin Fink, CTO of Western Digital, explains why Western Digital is using this open architecture. An eeNews report from the RISC-V Workshop in Barcelona.

Western Digital Gives A Billion Unit Boost To Open Source RISC-V CPU

Kevin Krewell Contributor
Tirias Research
Dec 6, 2017, 02:46pm • 5,783 views • #NewTech

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WESTERN DIGITAL TO ACCELERATE THE FUTURE OF NEXT-GENERATION COMPUTING ARCHITECTURES FOR BIG DATA AND FAST DATA ENVIRONMENTS

San Jose and Milpitas, Ca - November 28, 2017

Western Digital & RISC-V

Western Digital to Use RISC-V for Controllers, Processors, Purpose-Built Platforms

by Anton Shilov on December 14, 2017 5:00 PM EST

Posted in Storage | CPUs | Arm | Western Digital | SanDisk | RISC-V | Esperanto Technologies

NEWS

DesignNews Article: Western Digital Transitions To RISC-V Open-Source Architecture For Big Data, IoT

DATE: **DECEMBER 6, 2017**

RISC-V, the open-source computer core architecture, will be getting a big push from Western Digital in the coming years as the company has pledged to transitioning its own consumption of processors to RISC-V. According to the company Western Digital ships over one billion cores per year, and plans to double that number. And if all goes according to plan, they will all be based on RISC-V.

LEADER INSIGHTS

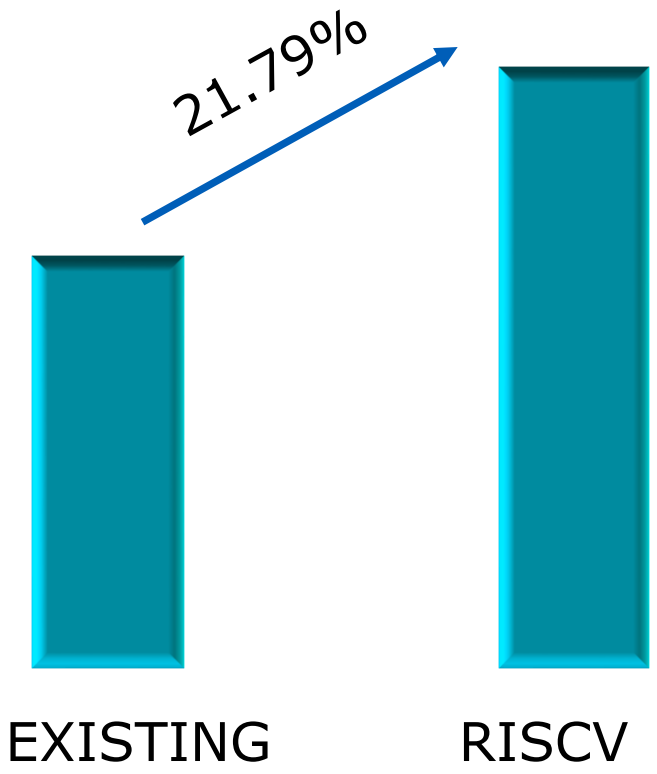
Big Data & Fast Data & RISC-V, Western Digital CTO Reveals the Connections

JoAnn Yamani | April 26, 2018 | no comment | Computing , GSA , Open Source , RISC-V , Semiconductor

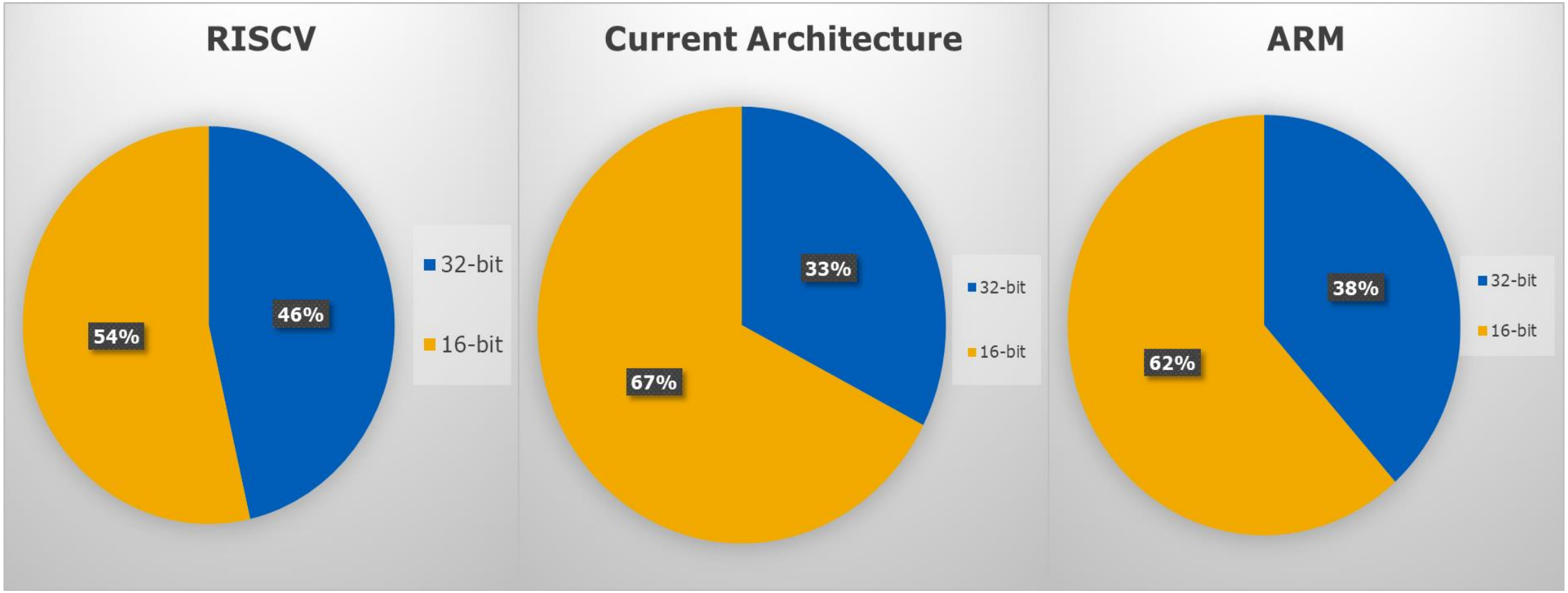
RISC-V ISA

- RISCV is an open architecture with fairly smaller Instruction Set.
- Focus is to study RISCV ISA and tool chain, targeting ultra-low cost embedded applications.
  - "C" extension(RV32IMC) chosen for the study which gives better code density on smaller system.
  - Standard Benchmarks used to study code density but they tend to be smaller. To get a broader view Storage Firmware was compiled and studied.
- Compare RISCV code density across architectures and provide recommendations for
  - ISA extensions.
  - compiler optimization.

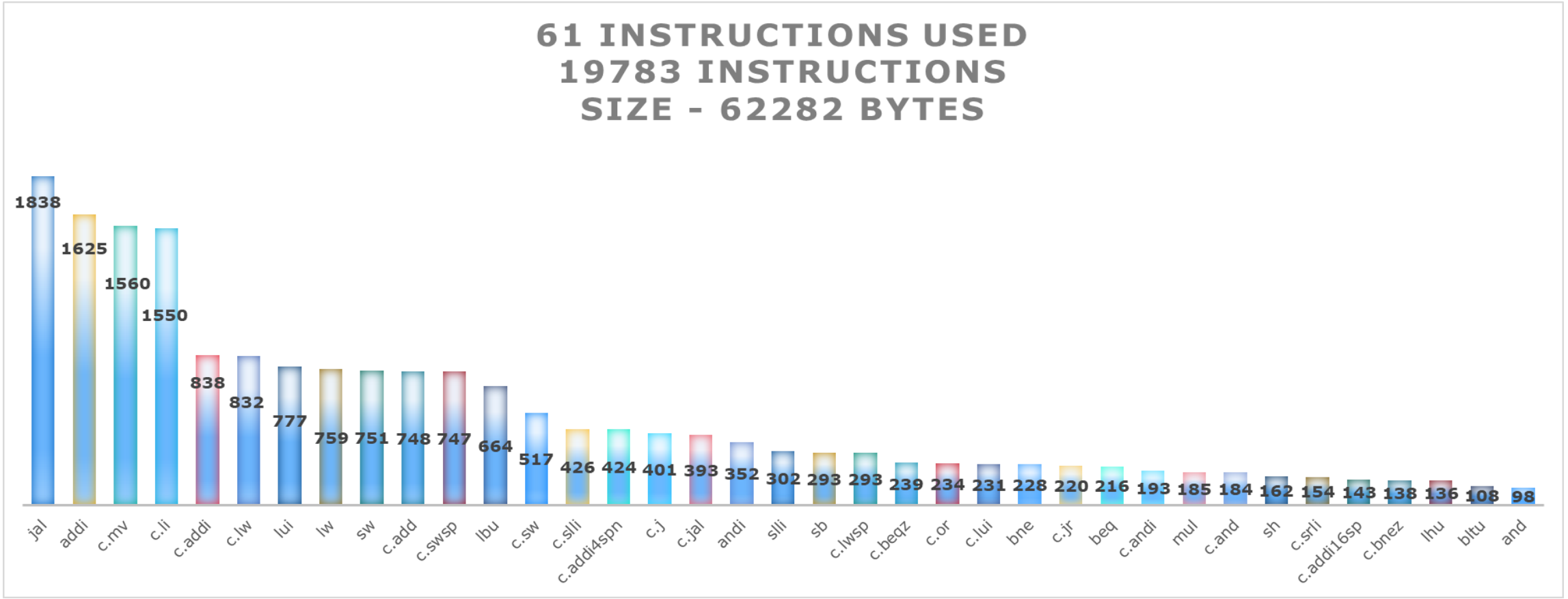
The problem…



Compressed Instruction distribution comparison.



RISC-V ISA distribution



High usage of “non”-compressed instructions in the top 10 instructions used!

Instruction under study

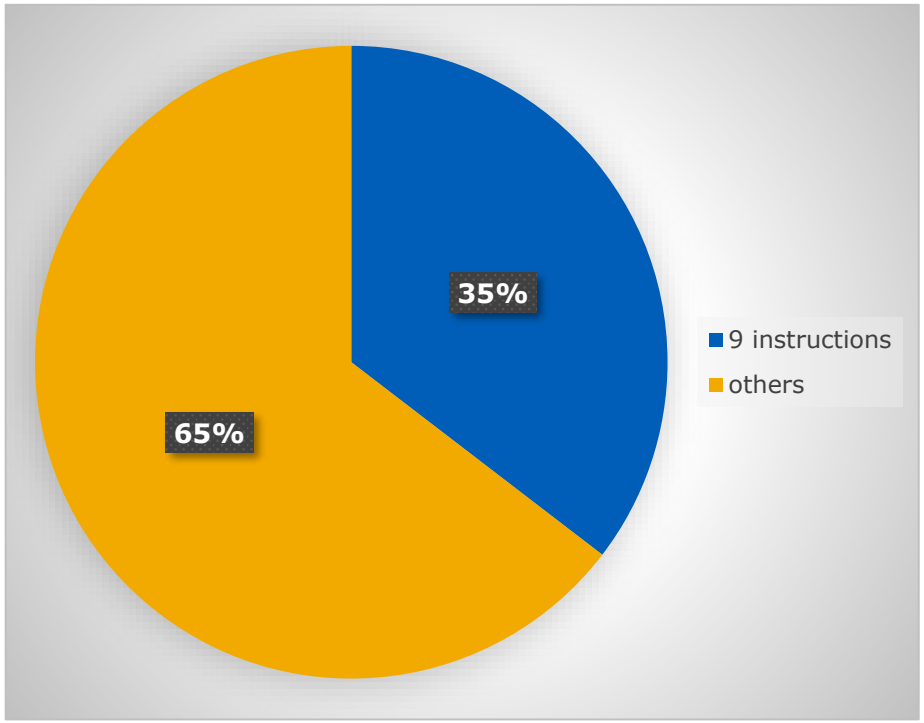
JAL

ADDI

LBU/SB

LHU/SH

LUI/LW/SW



ISA & Compiler Recommendations

Instructions	Usage Pattern (non 'C' Instructions)	Recommendation
ADDI	Heavily used to load immediate between 33 to 255	Compressed instruction to load 8-bit unsigned immediate
JAL	Heavily used to push/pop GPRs to/from stack	Compressed push/pop instruction
LBU/SB	load/store byte	Compressed instruction to load/store byte
LHU/SH	load/store half word	Compressed instruction to load/store half word
SLLI+SRLI	Half word assignments	Instruction to do zero extensions
LUI + LW/SW	Base loaded and non-compressed instruction used to load/store even in sequential memory accesses	Optimize compiler to Load closer base and use compressed load/store instructions
Macro compression	Currently No Macro compression	Implement Macro compression in compiler

Inference

- With the recommendations we can statically derive the code size reduction by analyzing the frequency of occurrence
- Code Size difference reduces from ~22% to ~3% with just these 6 patterns. With Macro compression and other patterns this gap can be closed even further
- Compressed instruction distribution also improves from **54% vs 46%** to **65% vs 35%**