Multi-Level Interrupt Design in RISC-V Linux

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Why do we need it ?

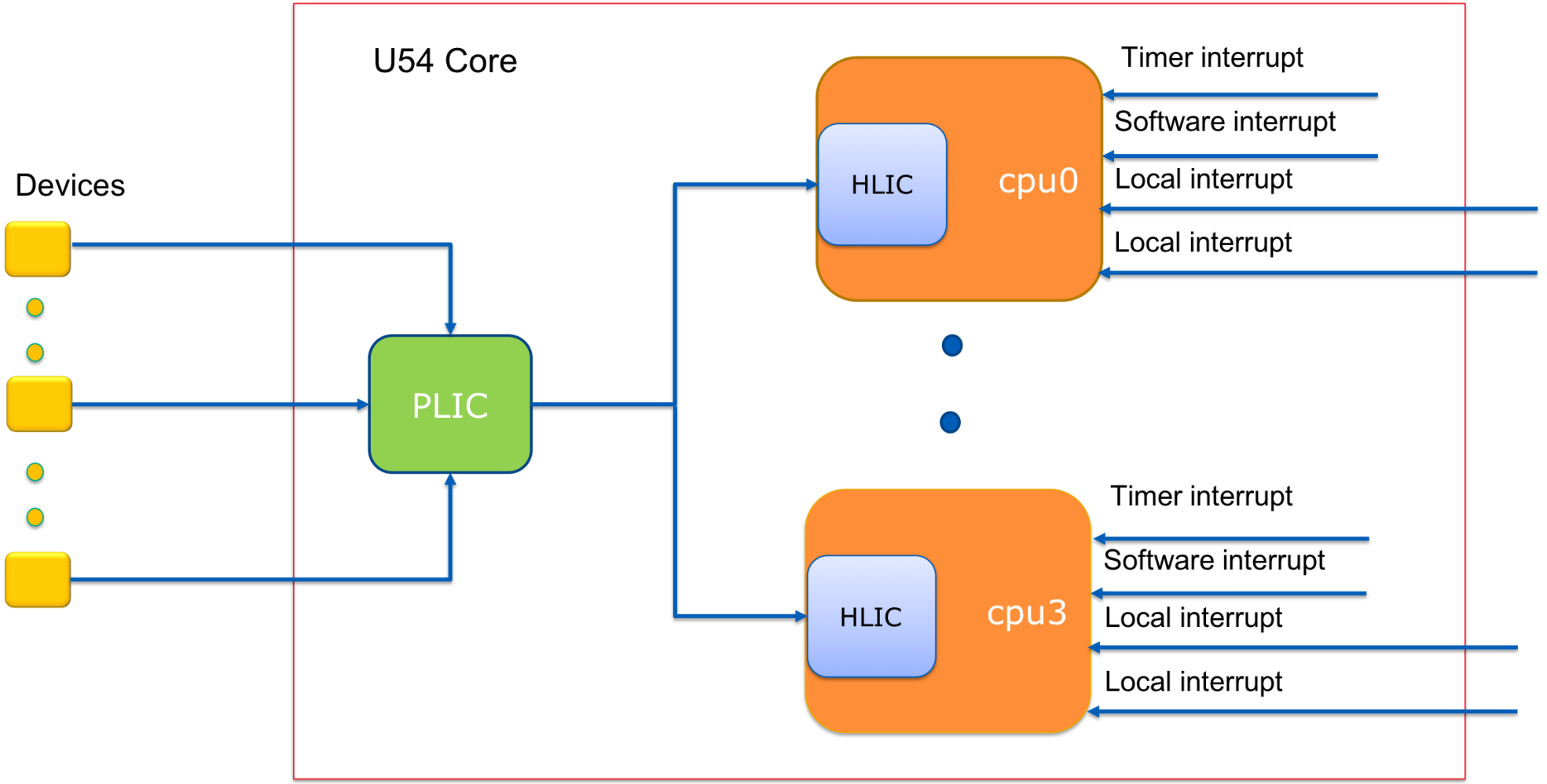
- Low Interrupt Latency is Key for high performant system

Design Choice	Pro	Con
Global Only	Multiplexing	Higher Interrupt latency
Local Only	Lower interrupt latency	Hardware complexity
Multi-level	Lower interrupt latency and multiplexing	Code complexity

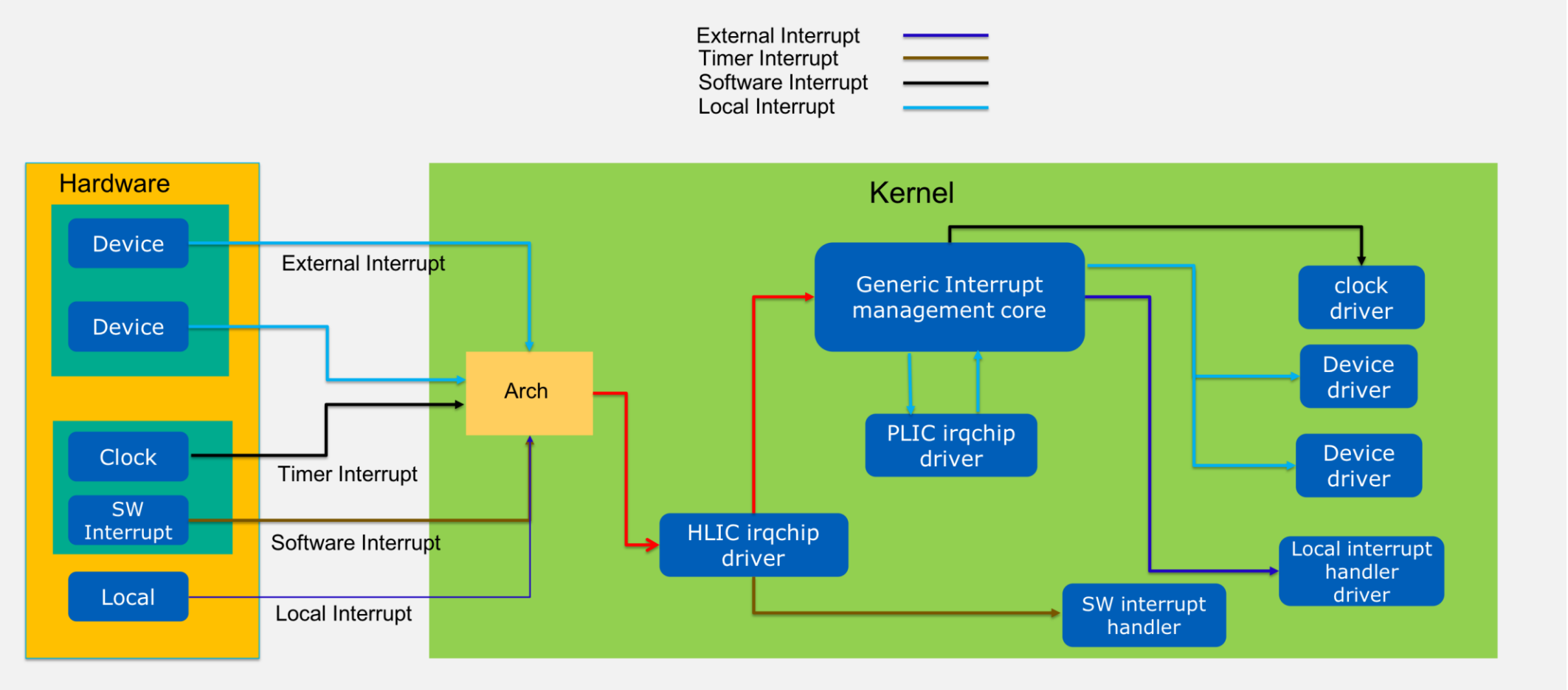
Interrupt Design in RISC-V

- Platform Level Interrupt controller (PLIC)
  - Centralized Interrupt prioritization & routing
  - Hart arbitration
  - Sends only a single external interrupt signal to hart
  - All external devices are connected to PLIC
- Local interrupts
  - Timer interrupt, Software Interrupt (Inter Processor Interrupts)
    - Core-Local Interruptor (CLINT) manages control & status registers in U54
    - Local interrupts (0-47) in U54
  - Connected to individual harts directly
  - Minimal latency

Linux view of RISC-V Hardware



Interrupt management design in Linux



See you at the Poster Session!!