

Processor Models and Tools + RISC-V Compliance verification



- Enable users to reduce embedded software schedules; improve software quality; achieve reliability, safety and security requirements; mesh with modern development methodologies such as Agile and Continuous Integration
- Key technologies
 - Instruction accurate simulation engines
 - Processor modeling methodology and library
 - Platform modeling methodology and library
 - Software development, debug, test and analysis tools
- RISC-V Models for Compliance verification
 - Check implementations to the RISC-V.org standards

RISC-V Processor Suite

- Processor models
 - RV32/64 GCN, RV32EC
 - Andes N25, NX25 including custom instructions
 - SiFive Mi-V (RV32IMA), E31, E51, U54
 - Added capability to enable easy addition of custom instructions, registers, etc. to processor model via side library
 - Does not perturb known, validated model source
 - All Imperas tools supported for complete model
- Platforms
 - Various RV32 models booting FreeRTOS
 - Single core RV64GC booting Linux in under 5 sec
 - Quad core RV64GCN (SiFive U540 platform) booting SMP Linux in about 7 sec
 - <http://www.imperas.com/sifive-risc-v-u540-mc-virtual-platform-booting-smp-linux-being-debugged-with-imperas-multi-core>
- Imperas tool support for RISC-V
 - MPD debugger for heterogeneous, multiprocessor/multicore platforms and driver-peripheral co-debug
 - Verification, Analysis and Profiling (VAP) tools including tracing, profiling, code coverage, OS-aware tools, timing estimation (paper at Embedded World)

RISC-V Compliance Work

- Active member of RISC-V.org Compliance Working Group
 - Driving architecture of test environment
 - Providing infrastructure for better quality compliance tests
 - Working with Formal Model Working Group to develop device configuration file format

- Migrating internally developed tests to be useable in device compliance testing

- Working with customers' RTL developers to check the compliance of their devices to the RISC-V.org standards
 - Using Imperas simulation/modeling technology