



# Variable Precision RISC-V Co-processor for Scientific Applications

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Andrea Bocco[1]
Tiago Trevisan Jost[1] (Speaker)
Yves Durand[1]
Christian Fabre[1]
Florent de Dinechin[2]
Anca Molnos[1]
[1]CEA, LETI, Univ. Grenoble Alpes, 38000 Grenoble, France,
[2]INSA, Lyon, France.

Andrea Bocco, Tiago Trevisan Jost (Speaker), Yves Durand, Christian Fabre, Florent de Dinechin, Anca Molnos
E-mail: andrea.bocco@cea.fr, tiago.trevisanjost@cea.fr

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# MOTIVATION AND PROPOSAL

- **Challenge in Scientific Computing applications**
  - Increase application numerical stability
  - Ensure/control convergence of iterative algorithms
  - Compensate ill-conditioning issues
- **Solution**
  - Adaptive (variable) precision format to address these problems
- **Proposal**
  - Augment RISC-V with Variable Precision (VP) Support
    - **Co-processor** that supports a VP format
    - **ISA extension** for using the unit
    - And a **programming model** that enables users to generate code for the co-processor.

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Andrea Bocco, Tiago Trevisan Jost (Speaker), Yves Durand, Christian Fabre, Florent de Dinechin, Anca Molnos
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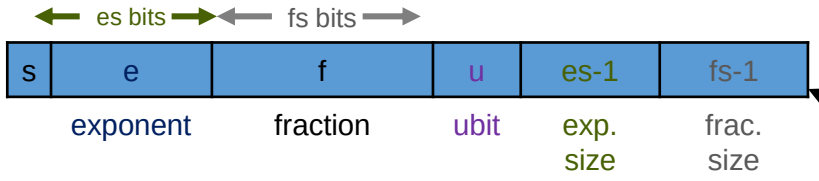
# PLATFORM FOR VP COMPUTING

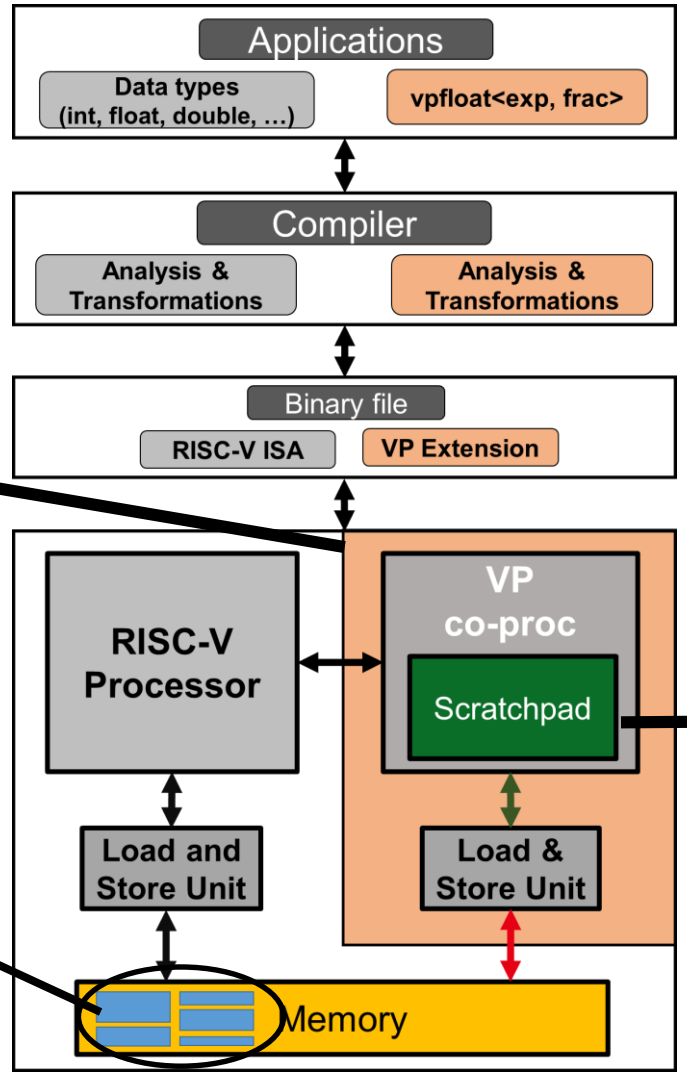
## VP Co-processor

- Co-processor implements the basic operations (add, sub, mul)
- Dedicated Load & Store Unit
  - Handles unaligned memory accesses
  - Keep memory footprint compact
  - Conversion between data memory format and register file format

## UNUM Format[4]

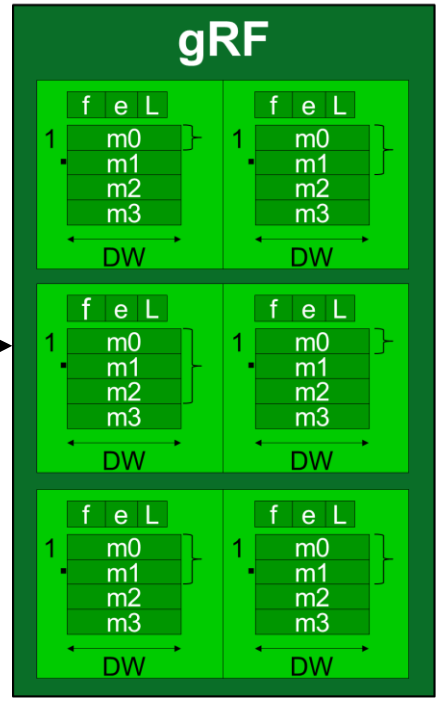
- "Metadata" fields for self-description of exponent and fraction sizes
- Ubit
  - FP number (0) or an open interval (1)




## ISA Extension

- ISA Extension
  - Set of instructions to manipulate VP numbers.



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# CONCLUSION

- **Augment RISC-V with VP FP Support**
  - A co-processor, an ISA, a programming model, and compiler support.
- **Work-in-progress**
  - Joined work between HW and SW group at our company
- **Future Works**
  - Measure power and energy consumption of the co-processor
  - Calling convention for the datatype
  - Full support from the compiler (middle-end optimizations, full backend support, object file generation, etc.)
  - Validation and experiments with real-life scientific applications.
- **References**


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