



# Mi-V RISC-V Ecosystem



**Mi-V**

™

# Agenda

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- RISC-V Primer
- Mi-V Ecosystem
  - RISC-V Soft Processor Offerings
  - Tools
  - Debug
  - Benchmarks
  - Kits
- Mi-V Ecosystem for Linux
  - Unleashed Expansion
  - Demo Machine Learning
- Summary

# What is RISC-V?

- A new, free, and open ISA developed at UC Berkeley
  - Using a permissible BSD license
- ISA is designed for
  - Simplicity: <50 instructions required to run Linux
  - Longevity: standardized instructions are fixed—your code runs forever
- RISC-V foundation set up to
  - Protect the ISA
  - Foster adoption
- RISC-V is not an open-source processor
  - Although open-source implementations will exist
  - Provides everyone an “architectural” license to innovate

# RISC-V Working Groups/Chairs

- Base ISA Ratification—Berkeley
- Bit Manipulation—AMD
- **Compliance—Microsemi/Codasip**
- **Debug—SiFive**
- **Formal Spec—Bluespec**
- Memory Model—NVIDIA, MIT
- Opcode Space Management—Berkeley
- Privilege Spec—SiFive
- SW Tool Chain—BAE
- **Vector Extensions—Berkeley, Esperanto Technologies**
- **Security—Nvidia**



**Bold = Microsemi Participation**

# Why RISC-V for Soft CPUs?

- Open-source ISA
  - Freedom to innovate at the micro-architectural level
  - Allows for RTL inspection—trust and certifications
  - Backed by industry leaders
- Longevity
  - Fixed ISA for long-term code portability
  - Easy migration to an ASIC
    - Without negotiating a license from ARM
- Proprietary/closed alternatives
  - ARM® Cortex-M1—encrypted RTL
  - NIOS (Intel) and MicroBlaze (Xilinx), licensed

***Open. Lowest Power. Programmable RISC-V Solutions.***

# Current SoC FPGA Offering

Features	SmartFusion ProASIC3, IGLOO	SmartFusion2 IGLOO2	PolarFire
Logic Elements	100–30K	5K–150K	100K–480K
Transceiver Rate		1 Gbps–5 Gbps	250 Mbps–12.7 Gbps
I/O Speeds	400 Mbps LVDS	667 Mbps DDR3 750 Mbps LVDS	1600 Mbps DDR4 1.6 Gbps LVDS
DSP (18x18 Multipliers)		240	1480
Max RAM	144 KB	5 MB	33 MB
Processor Option	100 MHz ARM Cortex-M3	Soft RISC-V 166 MHz ARM Cortex-M3	Soft RISC-V Crypto Co-Processor
On-Board Flash	Up to 512 KB code store	Up to 512 KB code store	56 KB secure NVM
Family Type	CPLD replacements Smallest packages	Low-density FPGAs with more resources and the lowest power	Mid-range density FPGAs Lowest power, cost optimized

## Hard Processor Subsystems, Soft RISC-V CPUs

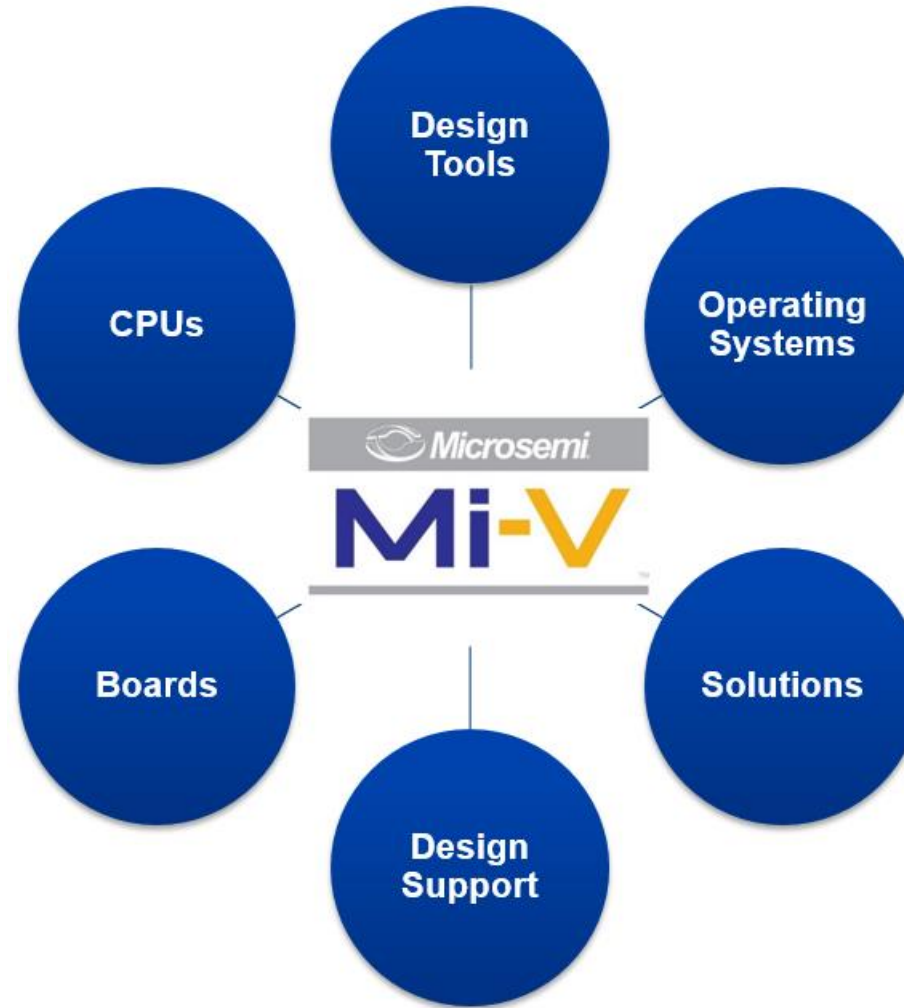


**Mi-V**<sup>TM</sup>

# Mi-V Ecosystem for PolarFire, RTG4, and IGLOO2 FPGAs

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# Mi-V Ecosystem Components



**A Comprehensive Ecosystem to Support RISC-V Development**

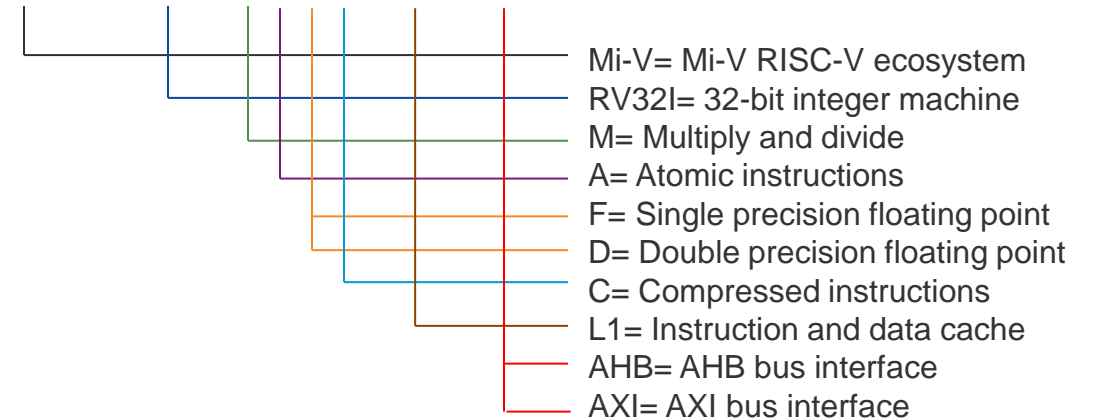


# CPUs: Mi-V Soft CPU Roadmap

Core	LEs	CoreMark	Cache	Mul/Div	Floating Point	Availability
CORE_RISCV_AXI4	10K	2.01	8K I and D	Yes		Now
Mi_V_RV32IMAC_L1_AHB	10K	2.01	8K I and D	Yes		Now
Mi_V_RV32IMACF_L1_AHB	26K	2.01	8K I and D	Yes	Single Precision	Now
Mi_V_RV32IC_AHB	4K					Q2'18

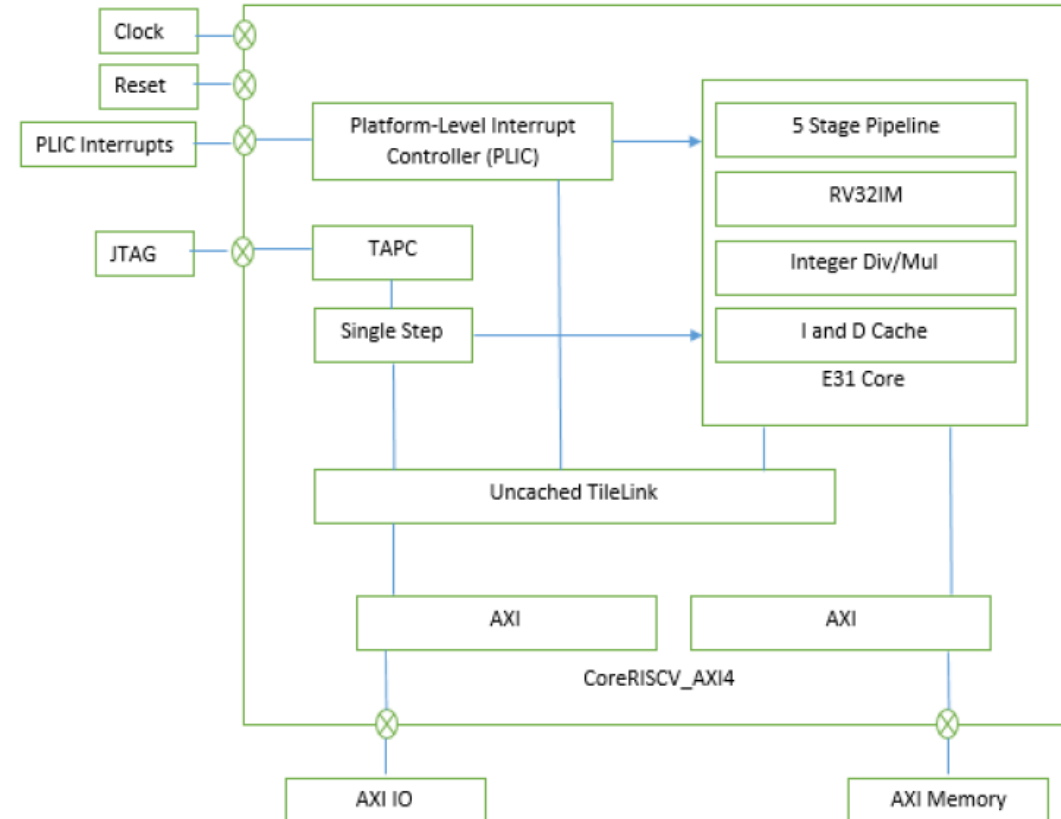
- New **Single Precision Floating Point** core being released now
- **Mi\_V\_RV32IC\_AHB**
  - Small core, without debug, estimate 4K LEs
- Additional cores to be added based on customer demand

Mi\_V\_RV32IMAFC\_L1\_AHB



# Mi-V RISC-V Soft CPU on PolarFire/RTG4/IGLOO2 FPGAs

- 5-stage pipeline
- 8K I/D cache
- Integer mul/div
- 2 breakpoints
- 31 interrupts
  - Priority by Int #
- 1.1 DMIPS/MHz
- 10K LEs
- 50 MHz–150 MHz
  - Depending on product



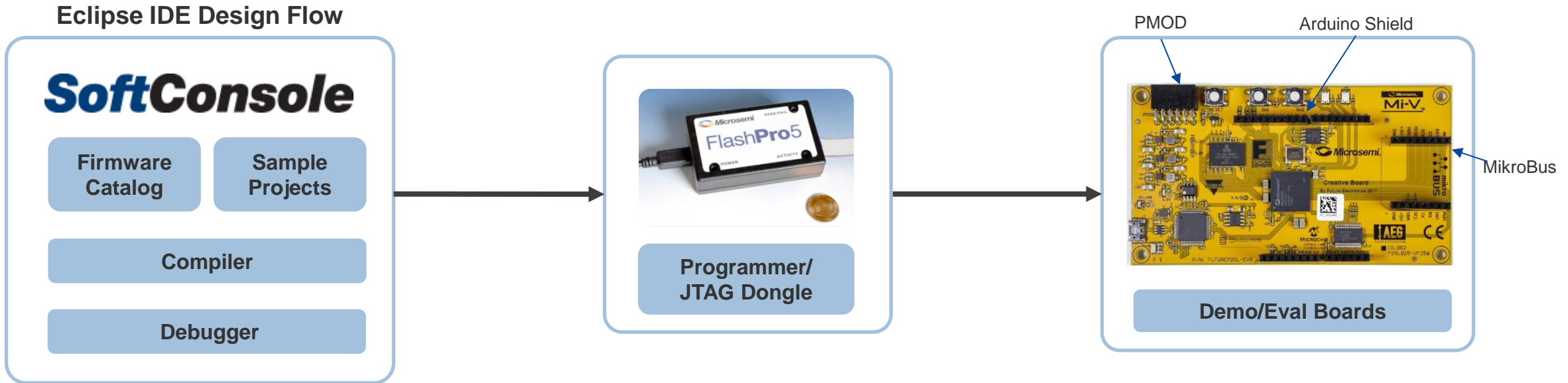
# Boot Sources for Mi-V RISC-V Soft CPUs

Product Family	Non-Volatile Source			
	On-Chip—Secure Boot (KB)			Off-Chip
	sNVM	uPROM	eNVM	SPI Flash
PolarFire	56	37–64		✓
RTG4		46		✓
IGLOO2			128–512	✓

sNVM    PUF-protected R/W NVM  
 uPROM   Read-only NVM  
 eNVM    R/W NVM

**The Only FPGA Supplier with Secure Boot Built-In and Open, Inspectable CPUs**

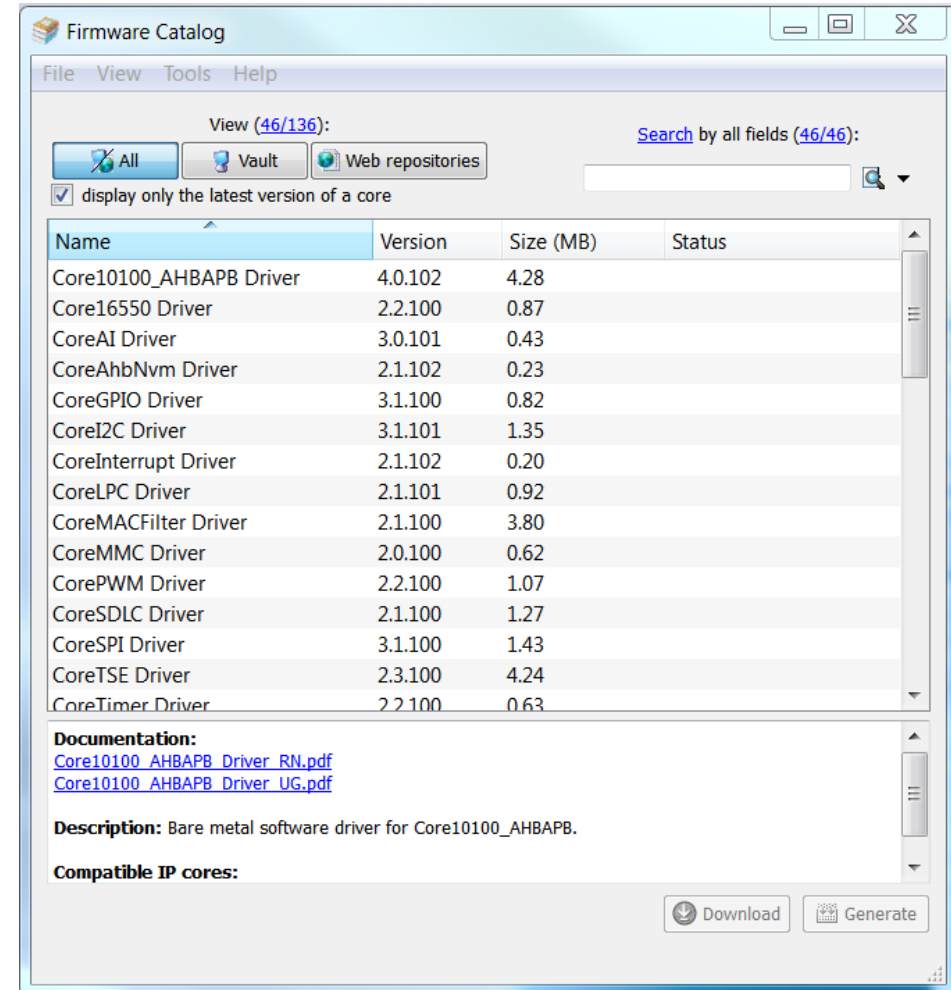
# SoftConsole Eclipse IDE



- A single tool chain for RISC-V and ARM MCUs
  - Easy migration from ARM to RISC-V
- Running on Linux or Windows hosts
- Supported by a Tier 1 supplier
- Bundled with example projects and RTOSs

# Firmware Catalog

- Drivers for Microsemi RISC-V soft CPUs
  - Updates pushed to your desktop
  - Release notes
  - User guides
- Version controlled
- MISRA/Netrino compliant



The screenshot shows the Firmware Catalog application window. The title bar reads "Firmware Catalog". The menu bar includes "File", "View", "Tools", and "Help". Below the menu bar, there are buttons for "All", "Vault", and "Web repositories", along with a search field labeled "Search by all fields (46/46)". A checkbox is checked with the text "display only the latest version of a core".

Name	Version	Size (MB)	Status
Core10100_AHBAPB Driver	4.0.102	4.28	
Core16550 Driver	2.2.100	0.87	
CoreAI Driver	3.0.101	0.43	
CoreAhbNvm Driver	2.1.102	0.23	
CoreGPIO Driver	3.1.100	0.82	
CoreI2C Driver	3.1.101	1.35	
CoreInterrupt Driver	2.1.102	0.20	
CoreLPC Driver	2.1.101	0.92	
CoreMACFilter Driver	2.1.100	3.80	
CoreMMC Driver	2.0.100	0.62	
CorePWM Driver	2.2.100	1.07	
CoreSDLC Driver	2.1.100	1.27	
CoreSPI Driver	3.1.100	1.43	
CoreTSE Driver	2.3.100	4.24	
CoreTimer Driver	2.2.100	0.63	

**Documentation:**  
[Core10100\\_AHBAPB\\_Driver\\_RN.pdf](#)  
[Core10100\\_AHBAPB\\_Driver\\_UG.pdf](#)

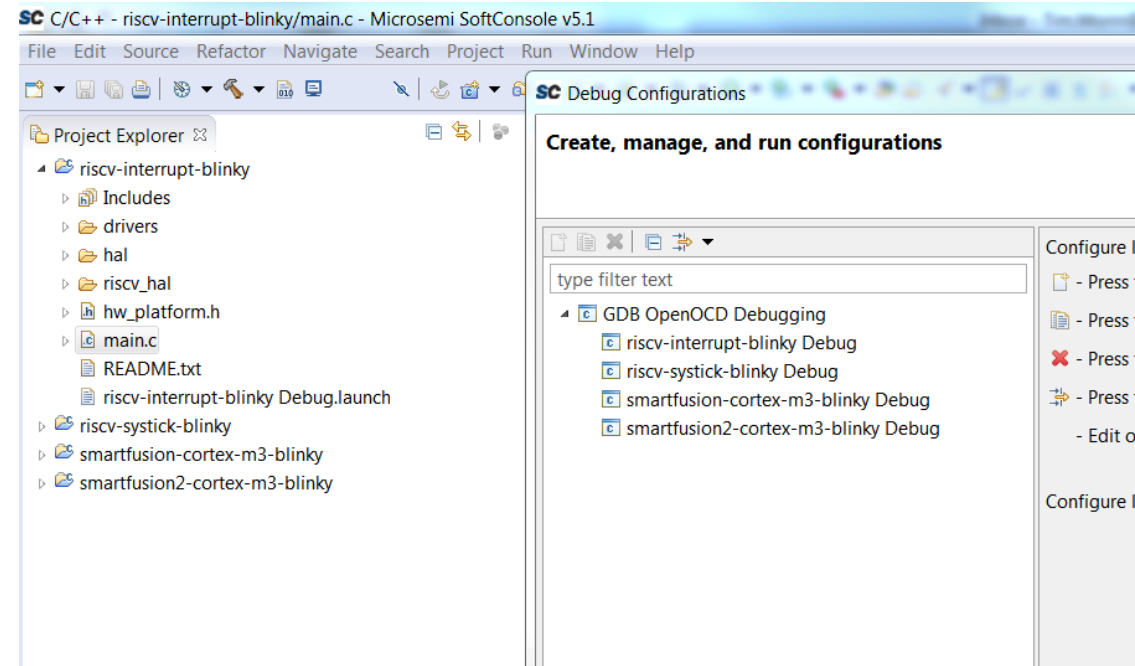
**Description:** Bare metal software driver for Core10100\_AHBAPB.

**Compatible IP cores:**

At the bottom right, there are "Download" and "Generate" buttons.

# Software Debug

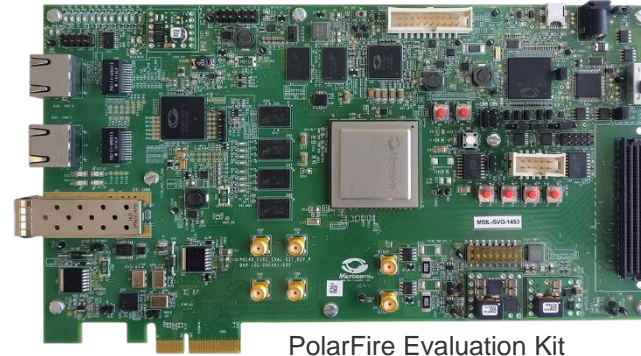
- Soft CPUs support 8 breakpoints
- GDB open OCD debug
- OpenOCD supports a wide range of dongles
  - FlashPro5
  - Olimex ARM-USB-TINY-H



# Boards: Mi-V Platforms

- Microsemi Soft CPUs on FPGAs

- PolarFire
- RTG4
- IGLOO2



PolarFire Evaluation Kit



RTG4 Development Kit

- SiFive Freedom Unleashed Platforms

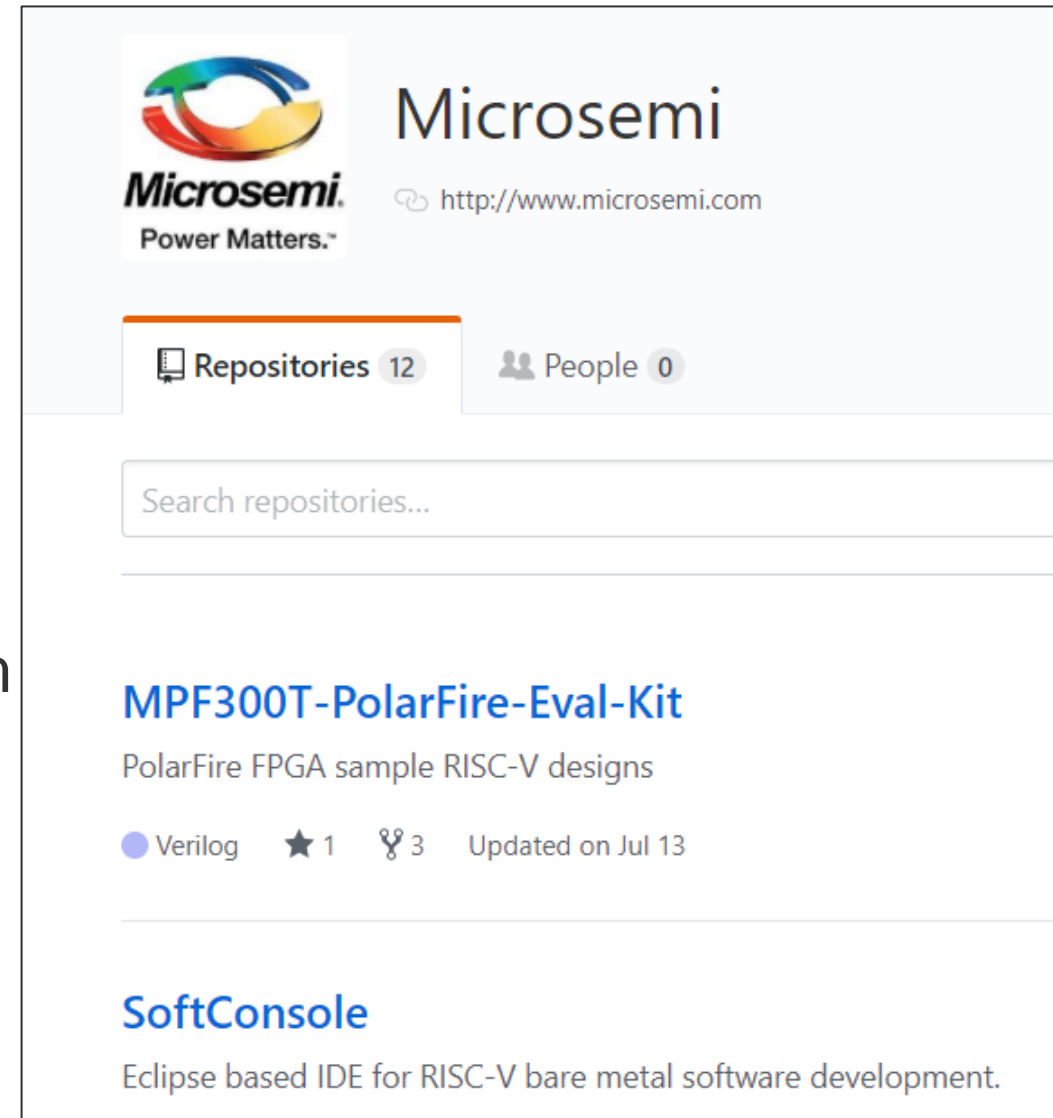
- HiFive1 FE310 Arduino platform validated with SoftConsole



Mi-V IGLOO2 Creative Development Board

# Solutions: Example Designs on Github

- Design examples targeted to various boards
  - Hello world printf through UART
  - Interrupt blinky
  - Touch screen tic-tac-toe
  - Crypto processor with RISC-V
- Getting started building a RISC-V tutorial
- RISC-V hardware abstraction layer to port from Cortex-M



The screenshot shows the GitHub profile for Microsemi. At the top left is the Microsemi logo with the tagline "Power Matters." and the website URL "http://www.microsemi.com". Below the logo, there are two statistics: "Repositories 12" and "People 0". A search bar labeled "Search repositories..." is positioned below these statistics. The first repository listed is "MPF300T-PolarFire-Eval-Kit", described as "PolarFire FPGA sample RISC-V designs". It has 1 star, 3 forks, and was updated on Jul 13. The second repository listed is "SoftConsole", described as "Eclipse based IDE for RISC-V bare metal software development."



# Operating Systems: Mi-V RISC-V Soft CPU RTOS Support

## ■ Open Source

- FreeRTOS
- Huawei LiteOS
- MyNewt
- Zephr (Hifive)



## ■ Commercial

- ExpressLogic—ThreadX
- SiLabs—Micrium  $\mu$ C/OSIII



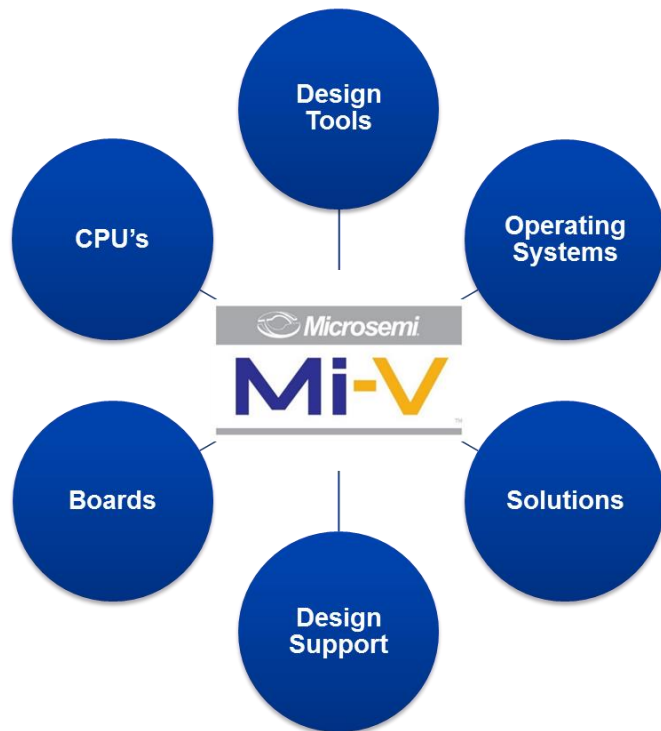
MicroPython

# Mi-V Supporting Linux

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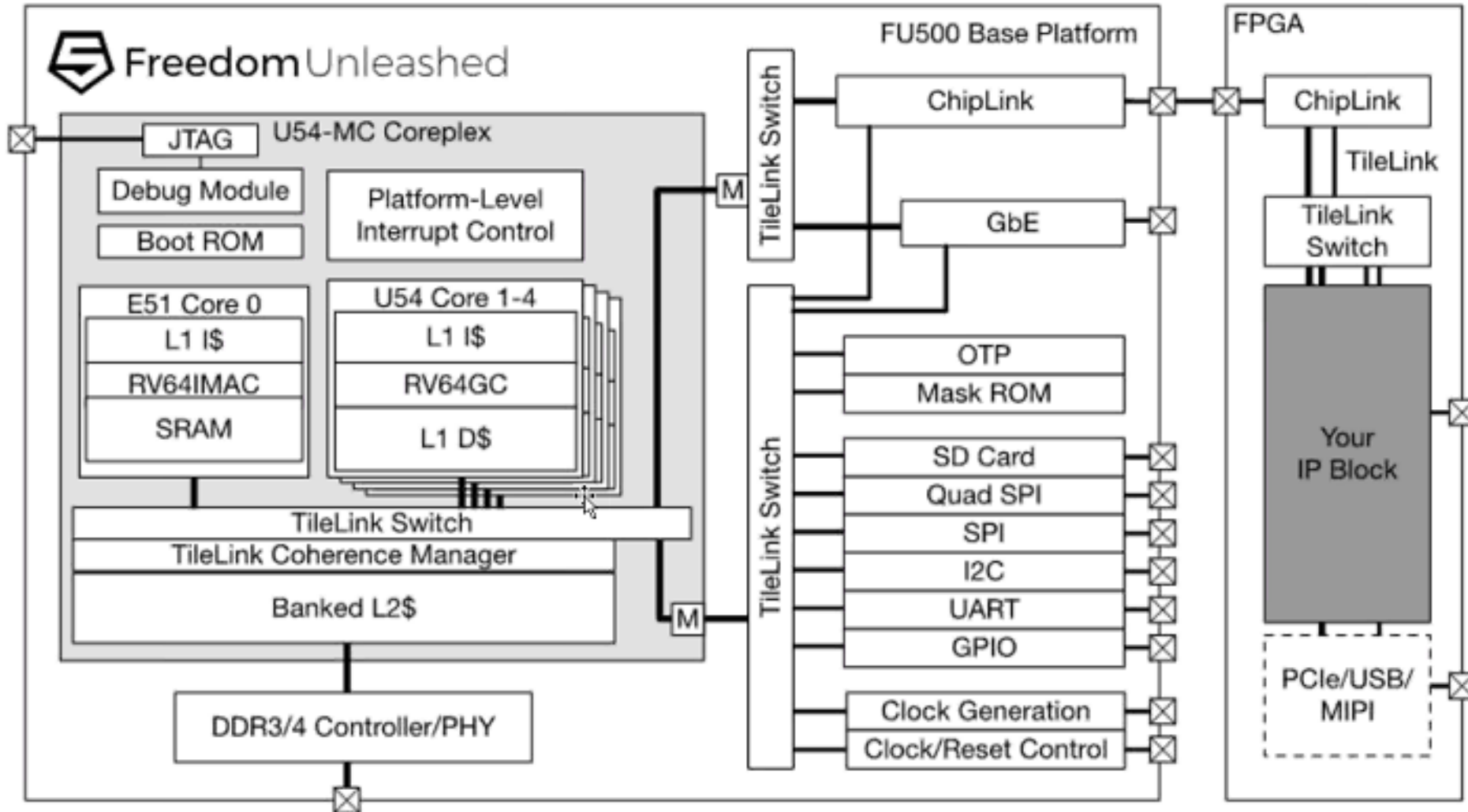
# Mi-V HiFive Unleashed Expansion: Advancing the Ecosystem

- Enables the community to port tools, OS's, middleware, packages to RISC-V
- Makes software development easier
- Enables standard and custom peripherals



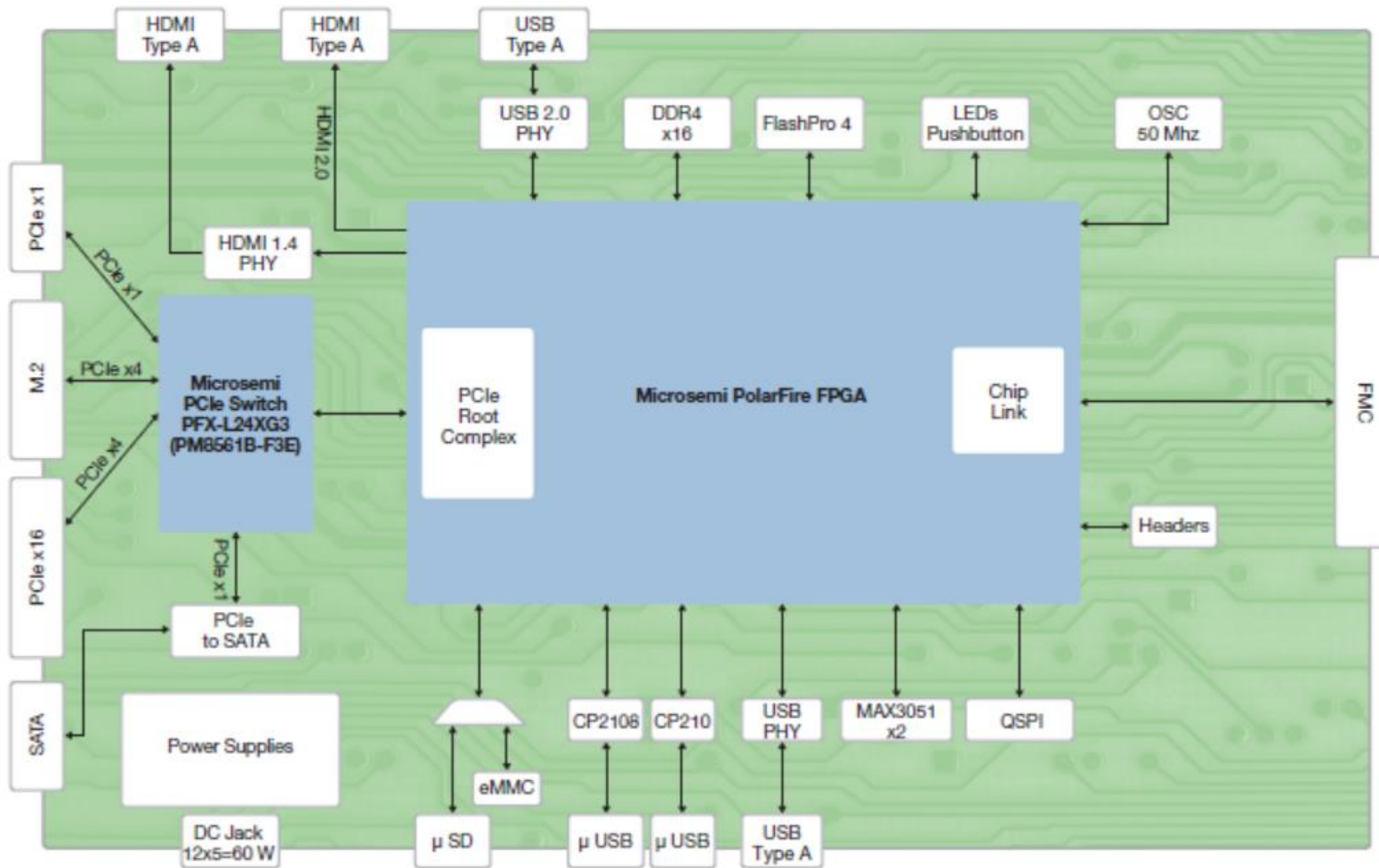
- Supporting the community supports our soft CPUs for our FPGAs
- Supporting the community supports the MI-V ecosystem and vice versa

# SiFive U-54 Block Diagram and Partnership



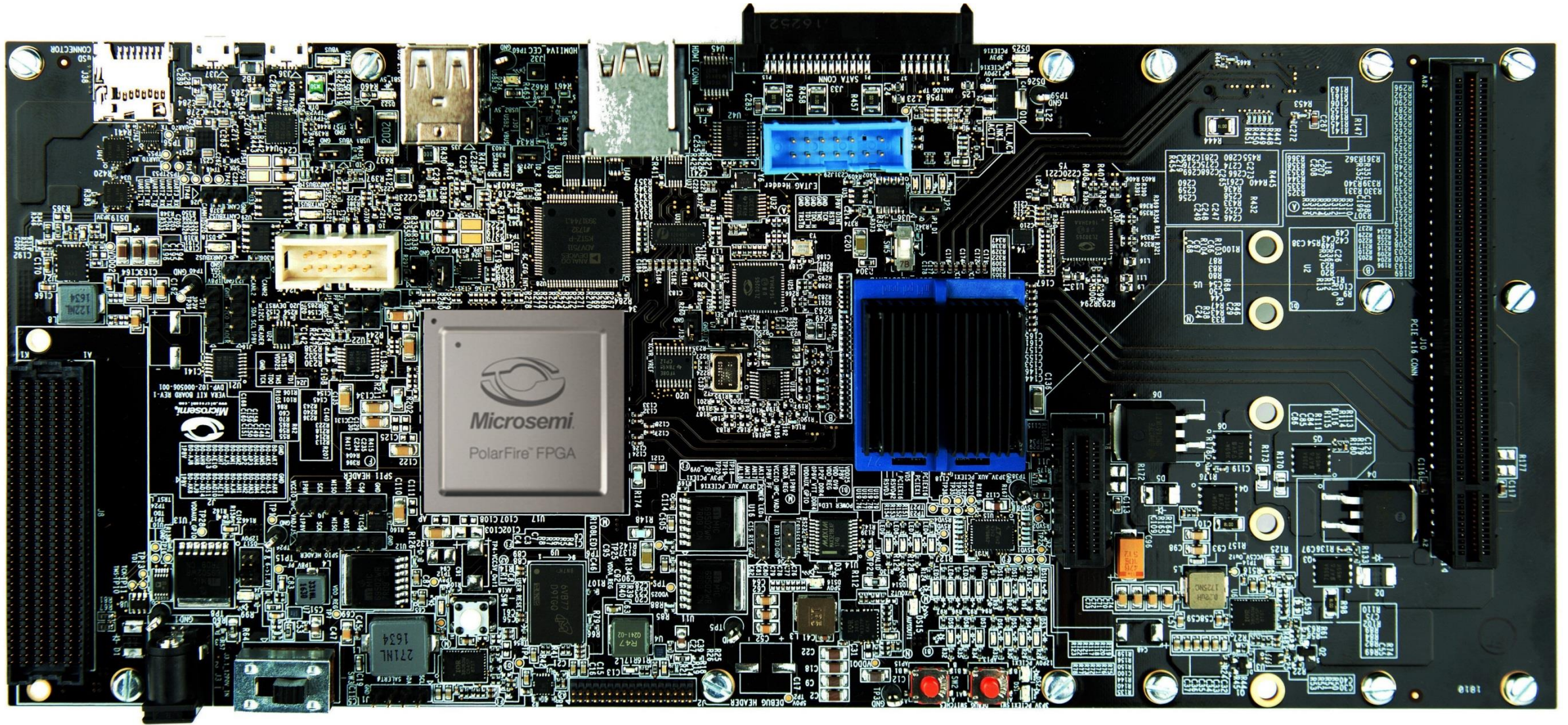
*TSMC Shuttle Run October*

# PolarFire HiFive Unleashed Development Platform

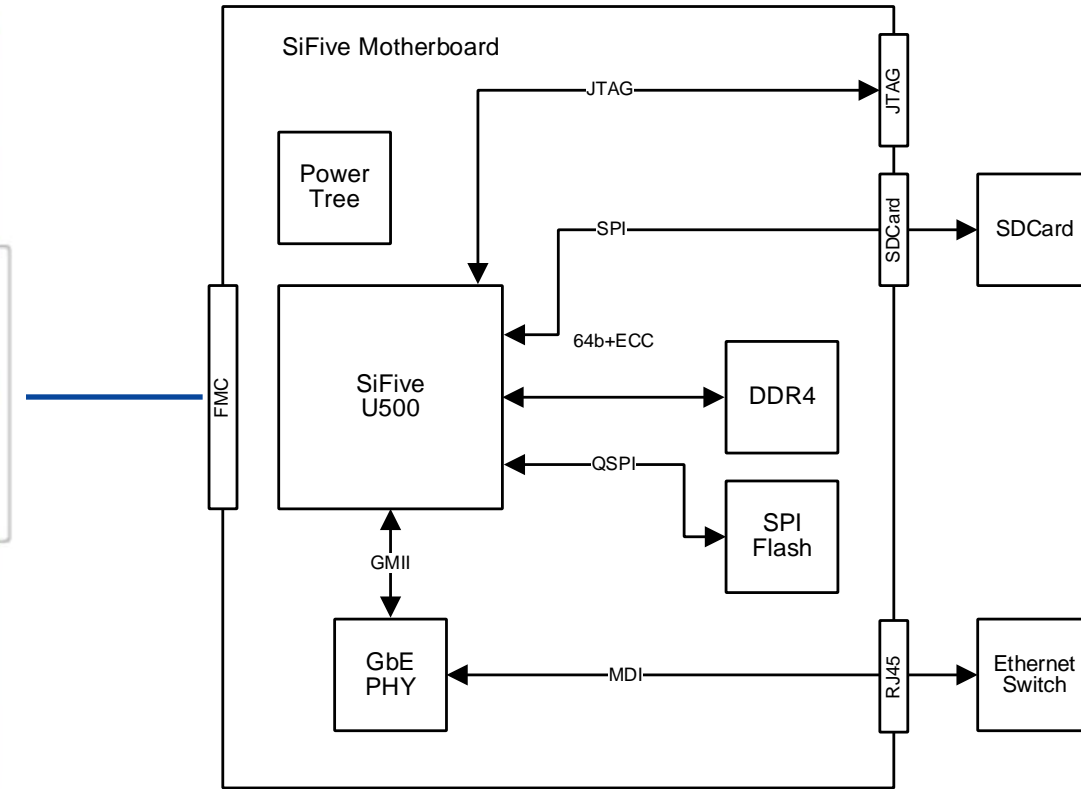
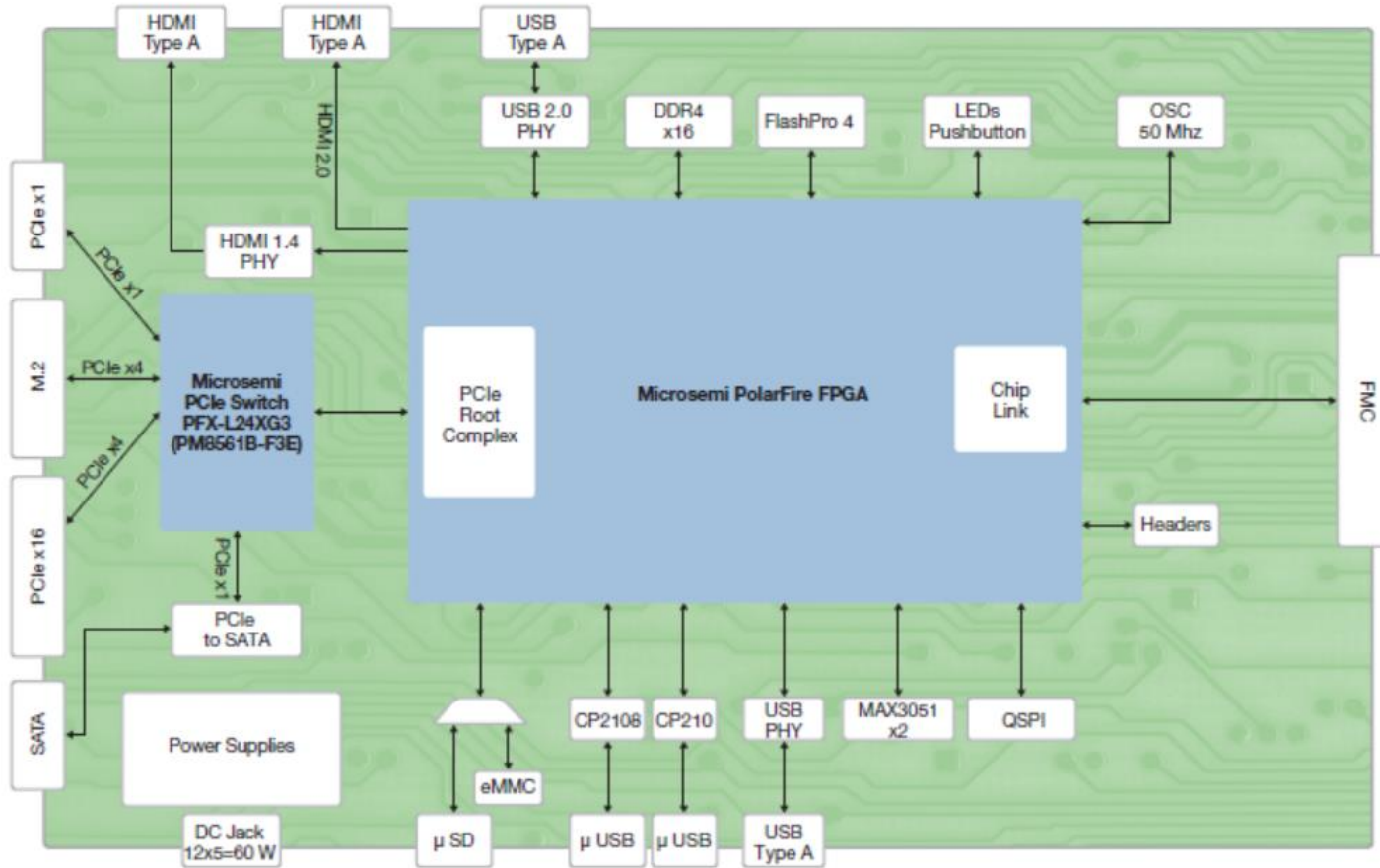


- Designed for Expandability
- Pre-programmed with a ChipLink to PCIe Root Port Bridge
- Enables Root Complex on the HiFive Unleashed Board
- Stay tuned for FPGA developer versions

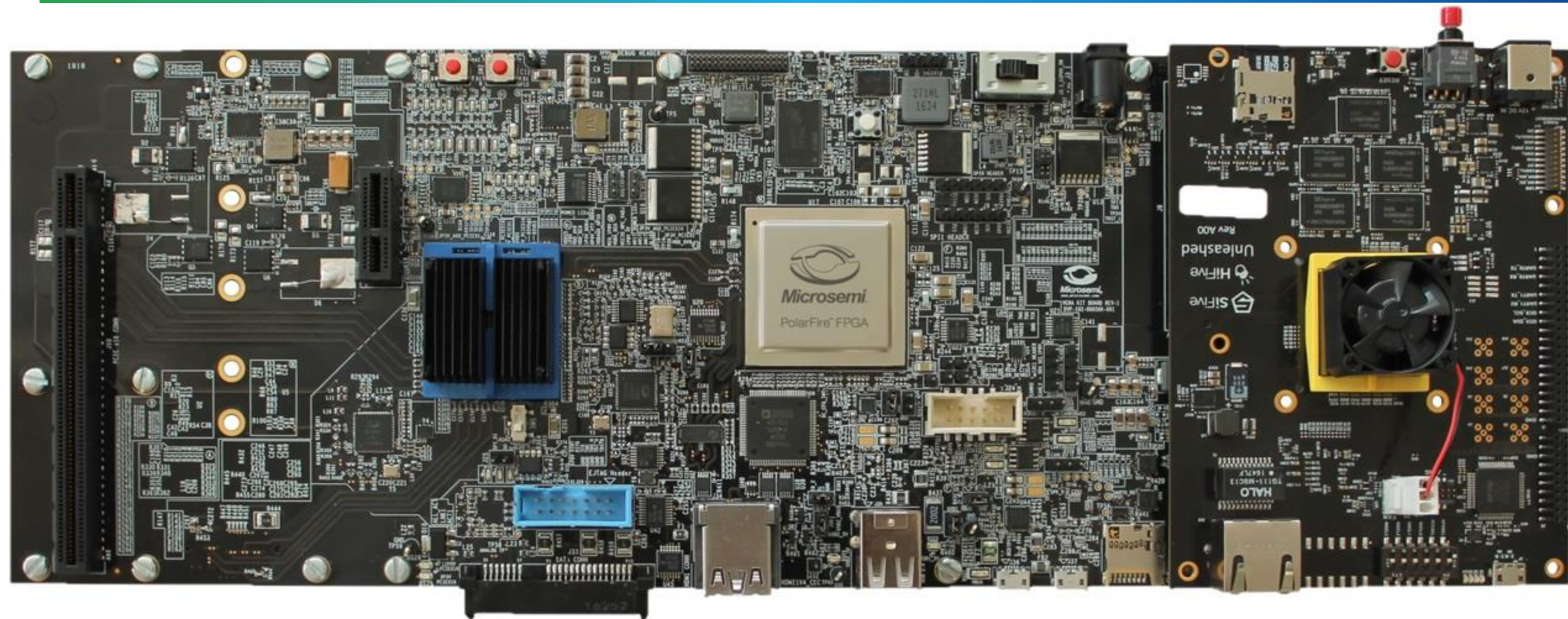
# Microsemi Mi-V HiFive Unleashed Expansion Board



# PolarFire Mi-V HiFive Unleashed Development Platform

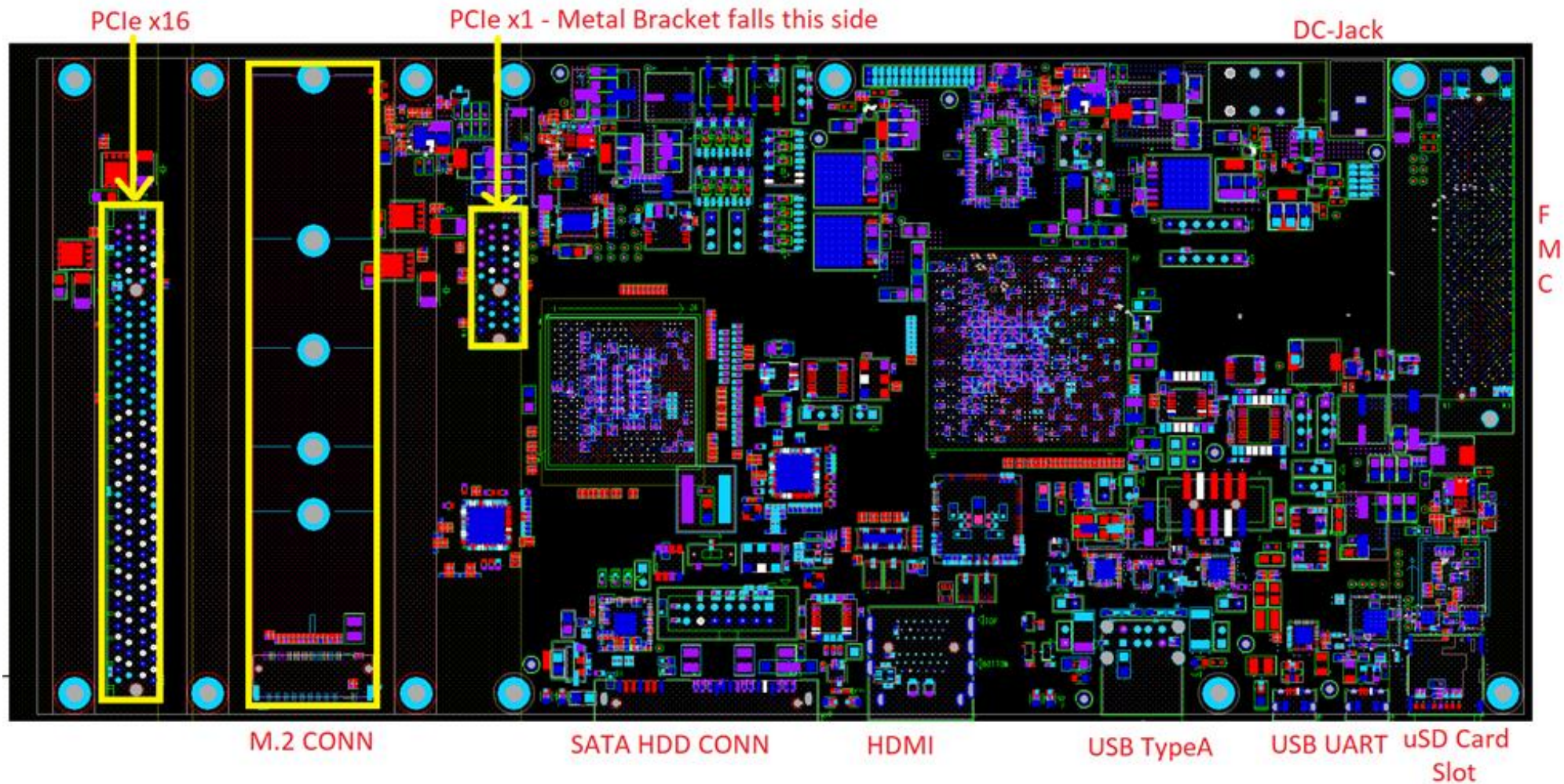


# HiFive Unleashed + Unleashed Expansion Board





# All the Peripherals You Need to Build a RISC-V PC

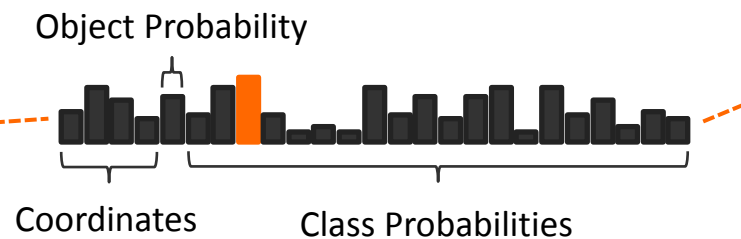
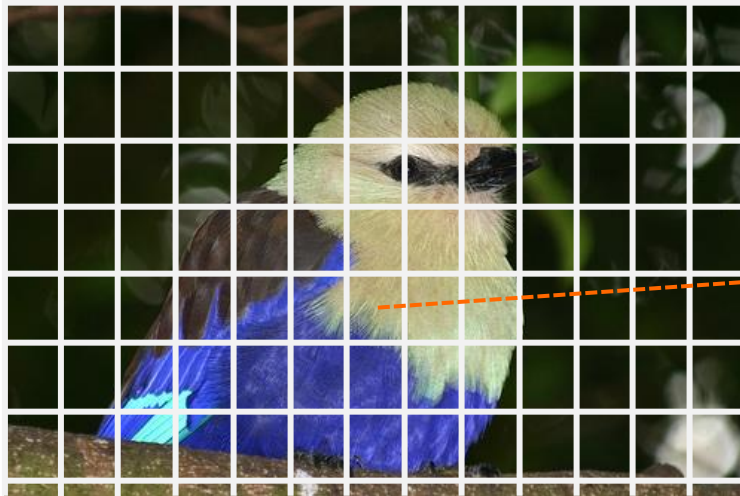


# ASIC Design Services – Deep Learning IP

## Tiny-YOLOv2

- Fully Convolutional Neural Network - 9 Convolutional Layers
  - convolution operation + batch normalisation + activation + pooling
- Trained end-to-end on Pascal VOC dataset
- Quantized and finetuned from provided base network by Joseph Redmon
  - Tiny YOLO @ <https://pjreddie.com/darknet/yolo/>

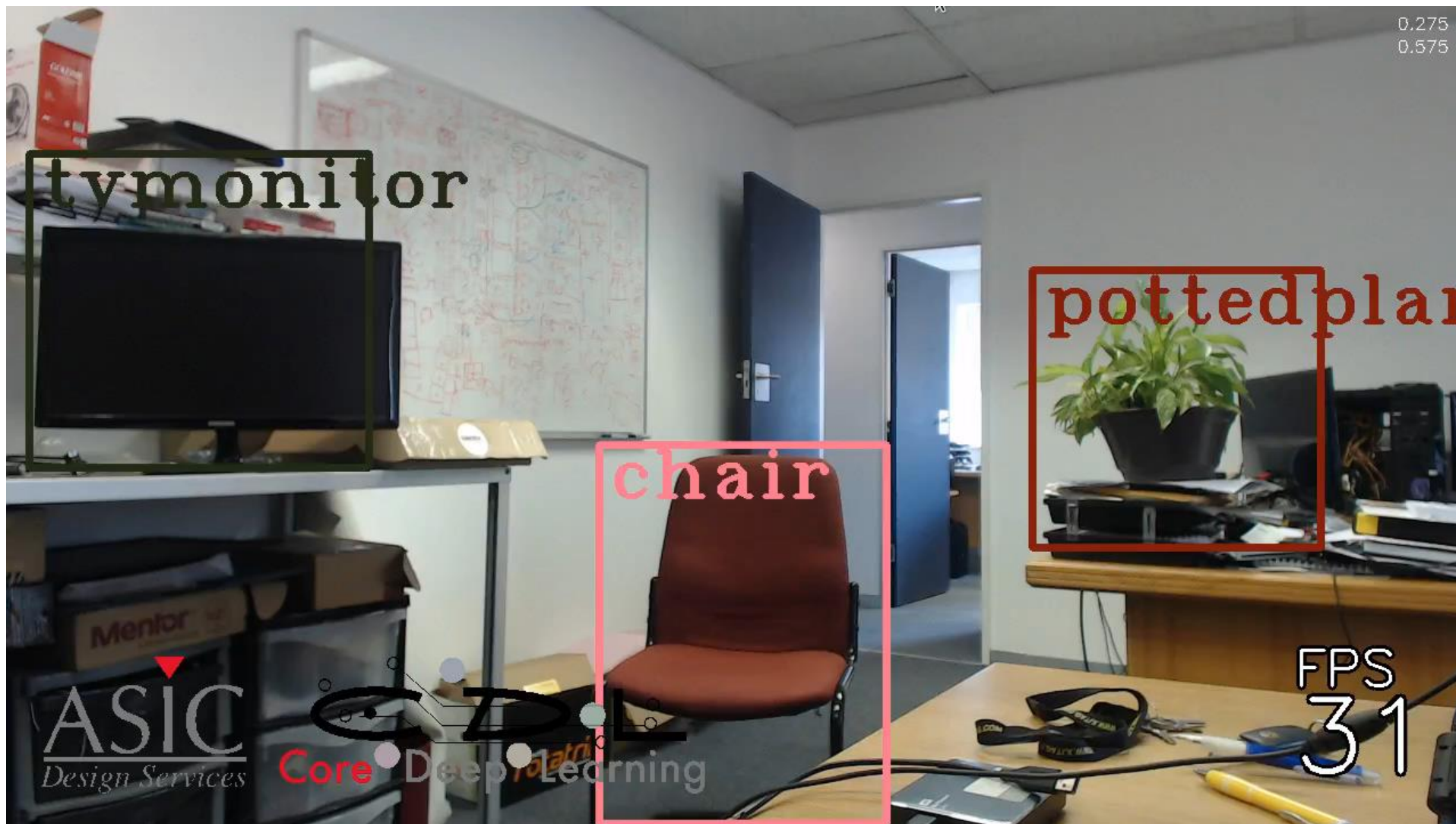
Core Deep Learning  
an embedded FPGA solution



Multiple predictions per grid location



# PolarFire Tiny Yolo Video

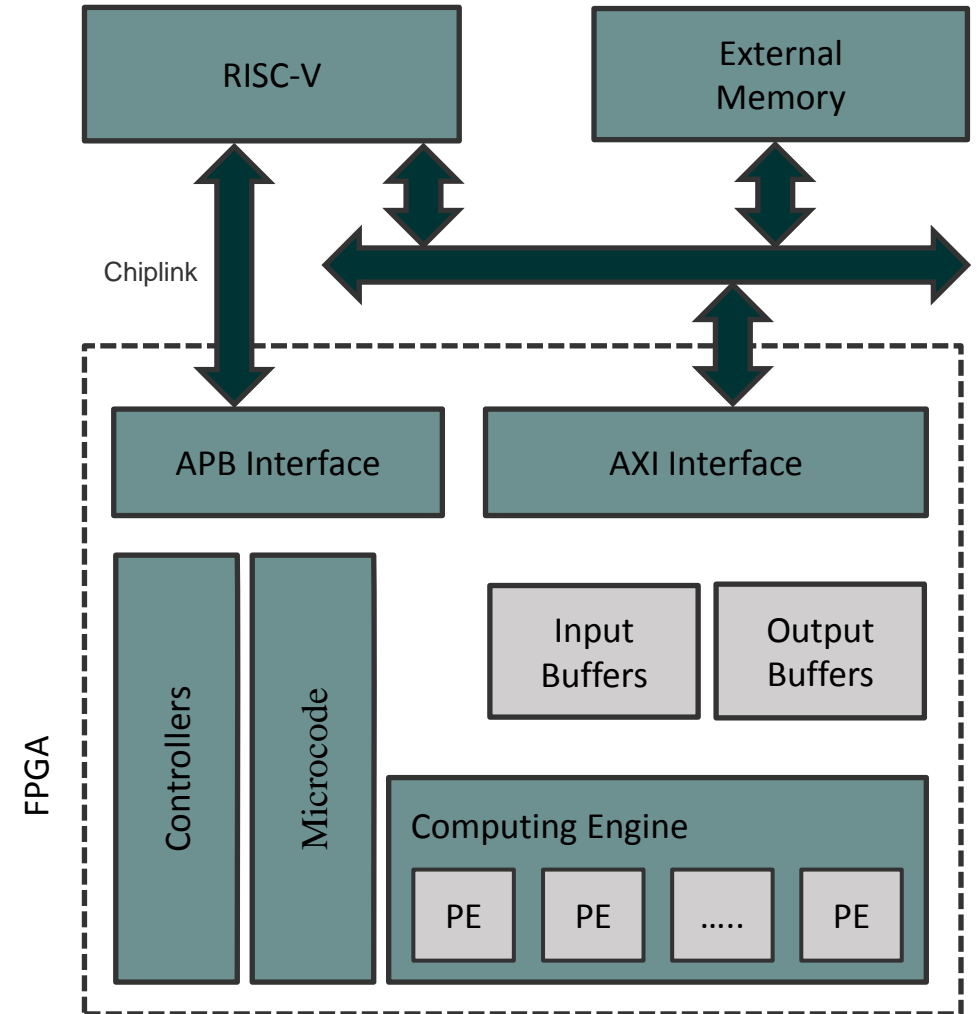


# Core Deep Learning Block Diagram

## Core Architecture

### Core generator features

- Full pipeline from convolutional neural network description to FPGA implementation
- Network retraining for memory footprint minimisation
- Support for different network layers
  - Convolutional layer
  - Fully connected layer
  - Pooling layer
  - Activation layers



# Mi-V RISC-V Soft CPU Summary

- A roadmap of soft CPUs for Microsemi FPGAs, royalty free
- Standardized ISA to protect your software investment
- Portable RTL for high-volume customers to migrate to an ASIC
- Security customers can inspect the RTL for trust
- Enables avionics and safety certification with viewable RTL
- Supported by industry-standard open-source tools



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# Mi-V HiFive Unleashed Expansion Summary

- Accelerates the RISC-V Linux Ecosystem
- Enable the community to port tools, OS's, middleware, packages to RISC-V
- Supporting the community supports our soft CPUs for our FPGAs
- Supporting the community supports the MI-V ecosystem and vice versa
- Deep Learning Core demo uses
  - Debian Linux, Xserver, OpenCV, V4L, PCIe and more were used

# Thank You



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