



Introducing the Newest SiFive RISC-V Core IP

E2 Series

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VP Product

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SiFive RISC-V Core IP Product Offering

SiFive RISC-V Core IP

E Cores

Industry leading 32-bit and 64-bit Embedded Cores

 **E3/5 Series**
High Performance Embedded

Networking
Industrial
Modems

 E51 Standard Core
 E31 Standard Core

 **E2 Series**
SiFive's Most Efficient Series

Microcontrollers
IoT
Wearables

 E21 Standard Core
 E20 Standard Core

U Cores

High performance 64-bit Application Cores

 **U5 Series**
Multi-Core RISC-V Linux

Low Cost Linux
Storage
Gateways


 U54-MC Standard Core

Core Series offer unique design points which can then be customized to meet application specific requirements

Standard Cores represent pre-configured implementations of a Core Series which are available for free RTL and FPGA evaluations



SiFive E3 and E5 Series RISC-V Core IP

 **E3/5 Series**
High Performance Embedded

Networking
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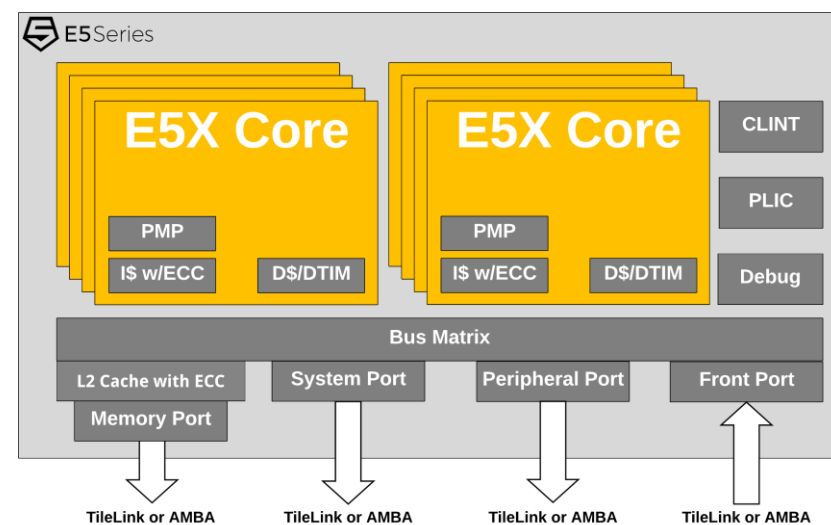
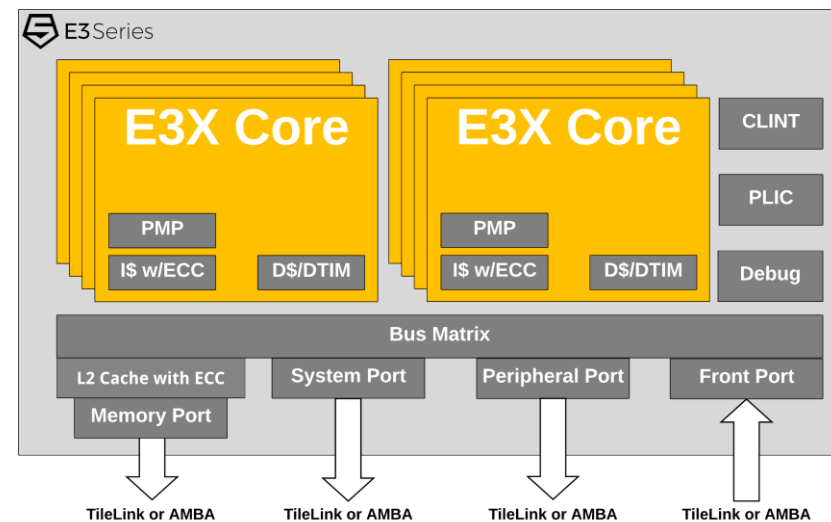
 **E51 Standard Core**
 **E31 Standard Core**



SiFive E3 and E5 Series Overview

High Performance 32bit and 64bit RISC-V MCUs

- **New Pipelined Multiplication Unit**
 - Better performance: 3 Coremarks/MHz
- **Multicore Support**
 - Pre-integrated and verified by SiFive
 - Supports up to 8+ cores
- **Flexible Memory Architecture**
 - I-Cache can be reconfigured into I-Cache + ITIM
 - DTIM for fast on Core Complex Data Access (D-Cache option also available)
 - ECC/Parity Protection on all memories
- **Fast Interrupts**
 - Supports fast vectored local interrupts and shared global interrupts
 - E3/E5 with Interrupt Handlers in ITIM can enter a local interrupt ISR in as little as **10** cycles
 - Does not require separate integration with a separate interrupt controller
- **Memory Protection**
 - 8 region physical memory protection
 - Region locking





Introducing SiFive E2 Series RISC-V Core IP

 **E2 Series**
SiFive's Most Efficient Series

Microcontrollers
IoT
Wearables

 E21 Standard Core
 E20 Standard Core



SiFive E2 Series RISC-V Core IP

- **SiFive's Smallest, Lowest Power, Core Series**

- Clean sheet design from the **inventors** of RISC-V
- New interrupt controller enabling **fast** interrupt handling
- Support for Heterogenous MP with other SiFive Cores

- **E2 Series Configurability**

- **Core** – Tune the E2 for higher performance, or lower area
- **Security** – Support for Memory Protection and RISC-V Machine and User Modes
- **Memory Map** – Fully customizable memory map
- **Ports** – Flexibility in the number and types of ports
- And more – Interrupts, Debug and Trace, Memory Protection, Tightly Integrated Memory

- **E20 and E21 are Standard Cores within the E2 Series**

- Standard Cores are benchmarked with published Power, Performance, and Area
- RTL and FPGA **evaluations** are **available**

SiFive E2 Series RISC-V Core IP

E20 Core Complex

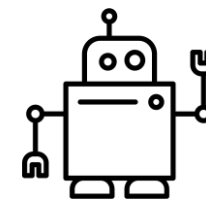
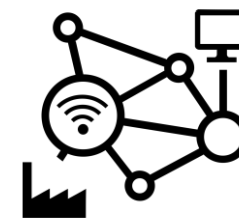
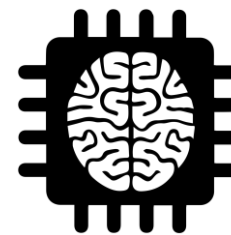
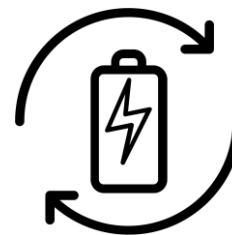
Industry leading 32-bit MCU efficiency:

- Embedded Microcontroller
- IoT
- Analog Mixed Signal
- 8-bit replacement
- Programmable Finite State Machine

E21 Core Complex

Full featured 32-bit RISC-V MCU :

- Sensor Fusion
- Wearables
- General Purpose Microcontroller
- Smart IoT
- Minion Core
- Smart Connected Toys

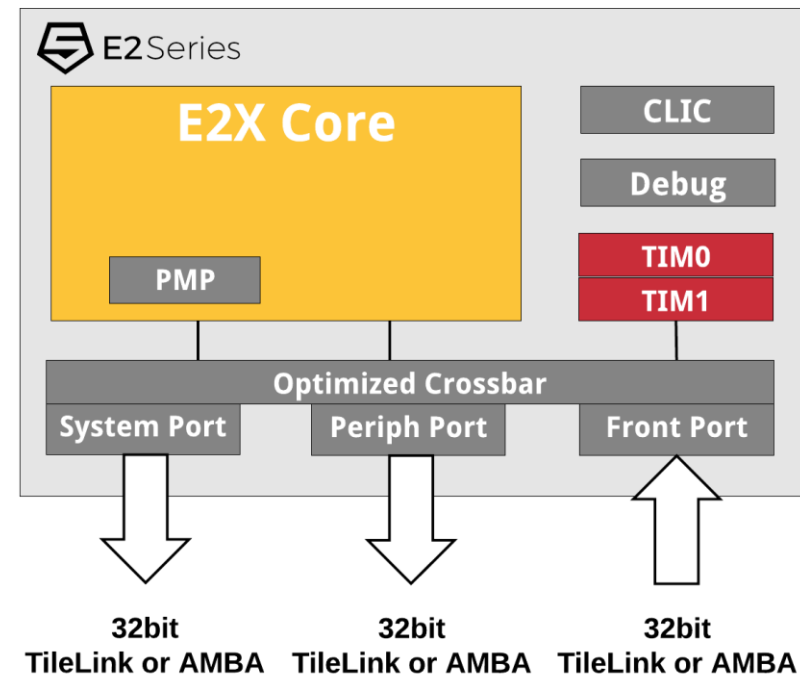




E2 Series Features

The Smallest, Most Efficient RISC-V MCU Family

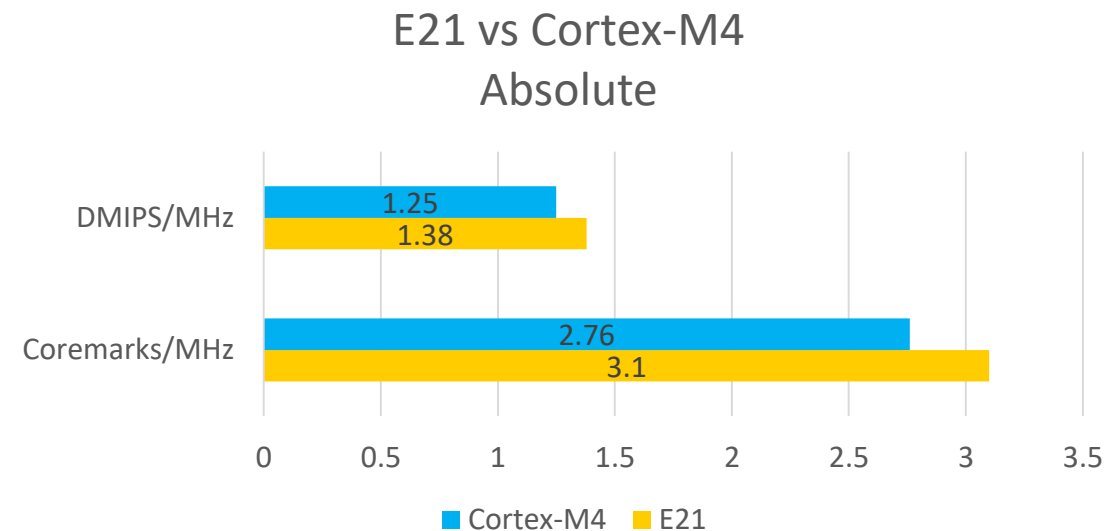
- **E2 Series core architectural overview**
 - RV32IMACF capable core
 - 2-3 stage, optional, Harvard Pipeline
- **Configurable to meet application specific needs**
 - Ability to add multiple outbound Ports of different specifications
 - Optional Tightly Integrated Memory (TIM)
 - Flexible address map
 - Optional FPU, tunable Multiply performance, Memory Protection, and more...
- **First RISC-V core with support for the RISC-V Core Local Interrupt Controller (CLIC)**
 - Execute first instruction of a C handler in **6 cycles**
 - Hardware interrupt prioritization and nesting
- **Drop In Cortex-M0+ and Cortex-M3/M4 replacement**
 - E21 has 12% more performance vs Cortex-M4
 - E20 has 28% more performance vs Cortex-M0+



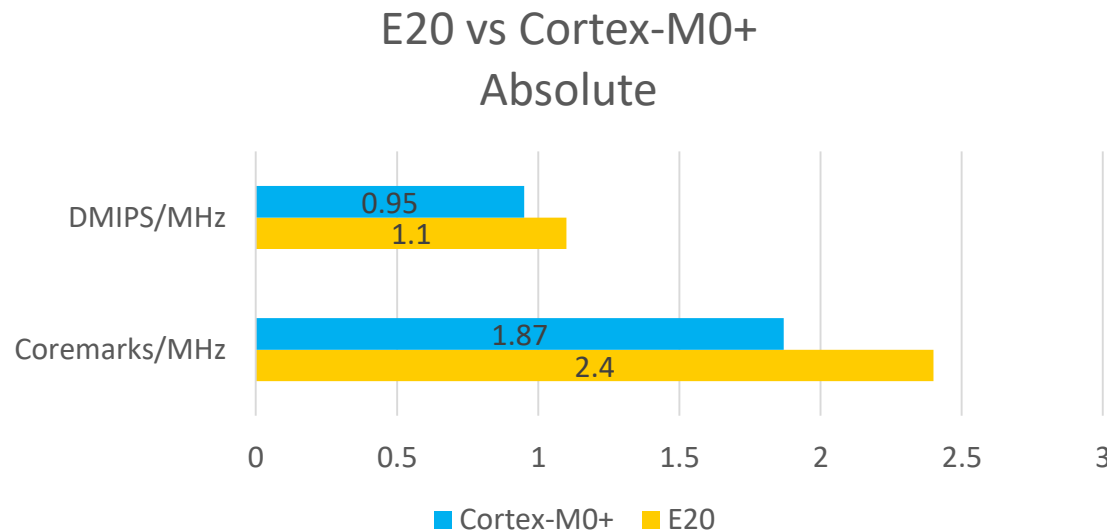


Better than the Competition

- **E21 is 12% higher performance per MHz vs Cortex-M4 in CoreMark**
 - When using equivalent GCC Compilers

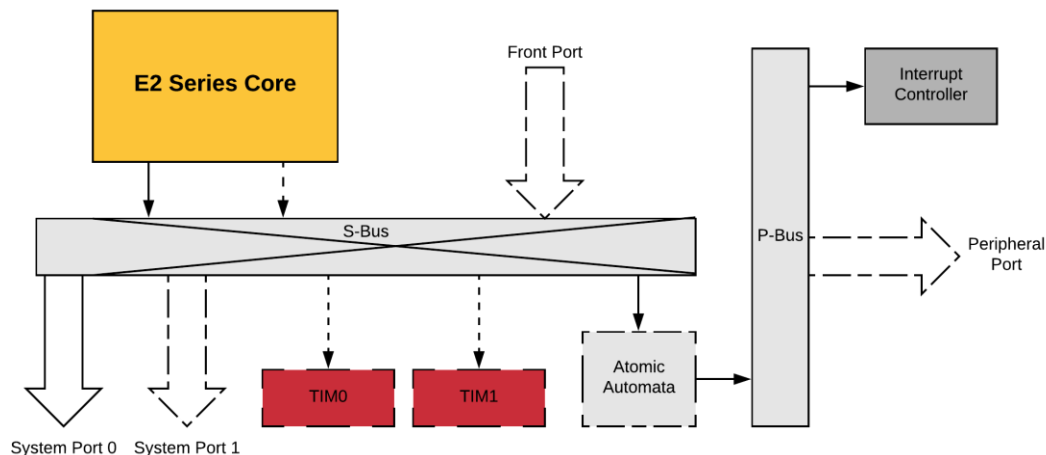


- **E20 is 28% higher performance per MHz vs Cortex-M0+ in CoreMark**
 - When using equivalent GCC Compilers





E2 Series Memory Subsystem



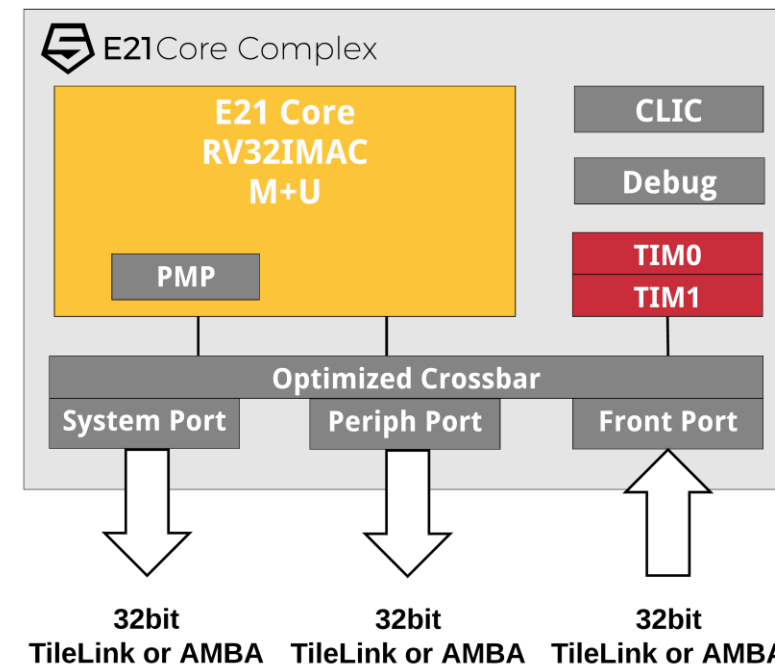
*Dotted lines represent optional interfaces/modules

- **E2 Core can be configured with 1 or 2 bus interfaces**
 - 2 bus interfaces allows for simultaneous Instruction and Data accesses from the core giving higher performance
- **S-Bus is a highly optimized crossbar allowing for fast access the TIM banks and System Port**
 - Can have multiple parallel access: Fetching instructions from one TIM, while writing data to the other
- **Optional 2x TIM banks**
 - Guaranteed low latency access through the S-Bus
 - Supports parallel access to both TIM banks for E2 cores with 2 bus interface configurations
- **P-Bus supports On-Core Complex peripherals and the Peripheral Port**
 - Support for RISC-V Atomic instructions which can be used for single-cycle Read-Modify-Write operations
- **E2 Core Instruction and Data accesses can target any Port or TIM**
 - No pre-defined address map! Place instructions and data where it makes sense for your application



E21 Standard Core

- **Full Featured RISC-V MCU**
 - 0.037mm² in TSMC 28HPC for entire Core Complex without TIM RAMs
 - 1.38 DMIPS/MHz, 3.1 Coremarks/MHz
- **2 Core Interfaces**
 - Allows for simultaneous instruction and data access
- **Efficient memory system**
 - Banked TIM for fast local memory
 - Simultaneous Instruction and Data Accesses (Harvard Architecture)
- **User Mode and Physical Memory Protection (PMP)**
 - 4 Region PMP
- **4 Hardware breakpoint/watchpoints**
- **Extreme low latency interrupt handling**
 - Execute first instruction of C handler in **6 cycles**
 - Execute entire ISR in **18 cycles**



E21 (AHB-Lite) Post-Route Physical Design				
	TSMC 28HPC		UMC 55LP	
Frequency @ worst setup corner	50MHz	585MHz	50MHz	210MHz
Worst Setup Corner	ssg_0p81v_m40c_cworst		ss_1p08v_125c_Cmax	
Implementation Details	9t; LVT, SVT, UHVT	12t; LVT, SVT, UHVT	7t; LVT, SVT, HVT	7t; LVT, SVT, HVT
Core Complex Area (mm ²)*	0.037	0.077	0.1	0.146
Core Only Area (mm ²)**	0.015	0.042	0.043	0.074
Core Complex Power – Dhrystone (mW) @ worst setup frequency	1.3	26	3.1	18
Power Characterization Corner	tt_0p9v_25c_typical		tt_1p2v_25c_Typ	

Note: All area and power numbers do not include RAMs

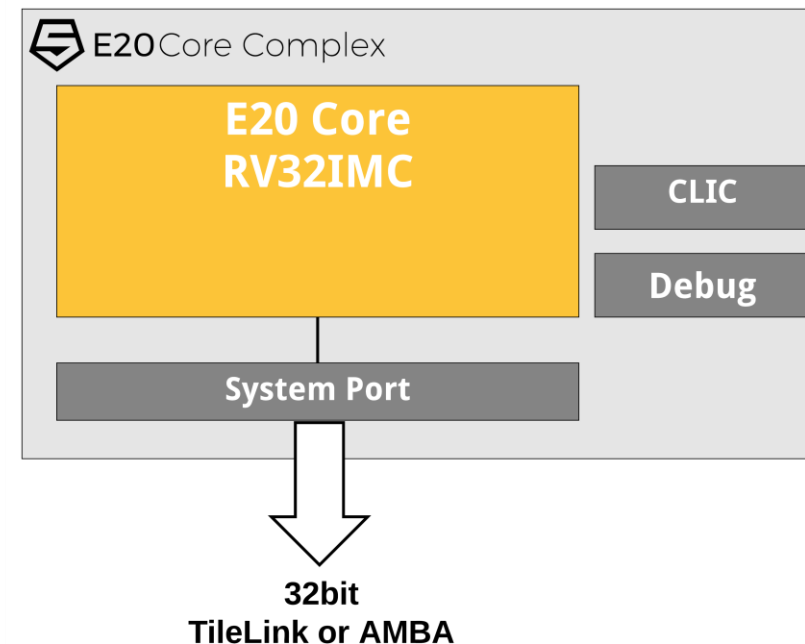
*Core Complex includes the Core plus CLIC w/127 irq and 4 priority bits, Debug w/ 4 hw breakpoints, 4 Region PMP, TIM Logic, internal bus and ports

**Core only includes the core pipeline only



E20 Standard Core

- **SiFive’s Most Efficient Standard Core**
 - 0.023mm² in TSMC 28HPC for entire Core Complex including CLIC, Debug, and System Port
 - 1.1DMIPS/MHz, 2.4 Coremarks/MHz
- **E20 Standard Core is optimized for Area and Power**
 - Single Core Interface for all Instruction and Data accesses
 - 4 cycle hardware multiply
 - Single System Port Interface
- **4 Hardware breakpoint/watchpoints**
- **Extreme low latency interrupt handling**
 - Execute first instruction of C handler in **6 cycles**
 - Execute entire ISR in **18 cycles**



E20 (AHB-Lite) Post-Route Physical Design				
	TSMC 28HPC		UMC 55LP	
Frequency @ worst setup corner	50MHz	725MHz	50MHz	250MHz
Worst Setup Corner	ssg_0p81v_m40c_cworst		ss_1p08v_125c_Cmax	
Implementation Details	9t; LVT, SVT, UHVT	12t; LVT, SVT, UHVT	7t; LVT, SVT, HVT	7t; LVT, SVT, HVT
Core Complex Area (mm ²)*	0.023	0.046	0.064	0.083
Core Only Area (mm ² **)	0.011	0.029	0.031	0.049
Core Complex Power – Dhrystone (mW) @ worst setup frequency	0.58	18	1.3	8.8
Power Characterization Corner	tt_0p9v_25c_typical		tt_1p2v_25c_Typ	

Note: All area and power numbers do not include RAMs

*Core Complex includes the Core plus CLIC w/32 irq and 2 priority bits, Debug w/ 4 hw breakpoints, internal bus and ports

**Core only includes the core pipeline only



Summary

- **SiFive has multiple different Series of RISC-V Core IP to cover all areas of computing**
 - Microcontrollers
 - Embedded
 - Application/Linux Cores
- **Standard cores for fast deployment, silicon proven IP**
- **Configuration options within Core Series to customize the core for your application**
- **RISC-V ISA has the promise to be the ISA for all types of computing – now we are seeing the implementations**



Join the Revolution

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