RISC-V: Opportunities and Challenges in SoCs

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Introductions

- Who am I?

- Why am I here?

Quick tour of an SoC

Quick tour of an SoC

Power-optimized CPU cluster

Perf-optimized CPU cluster

LTE modem

Crypto

Secure core

Sensors

DDR

Interconnect

GPU

Video

Camera

Audio

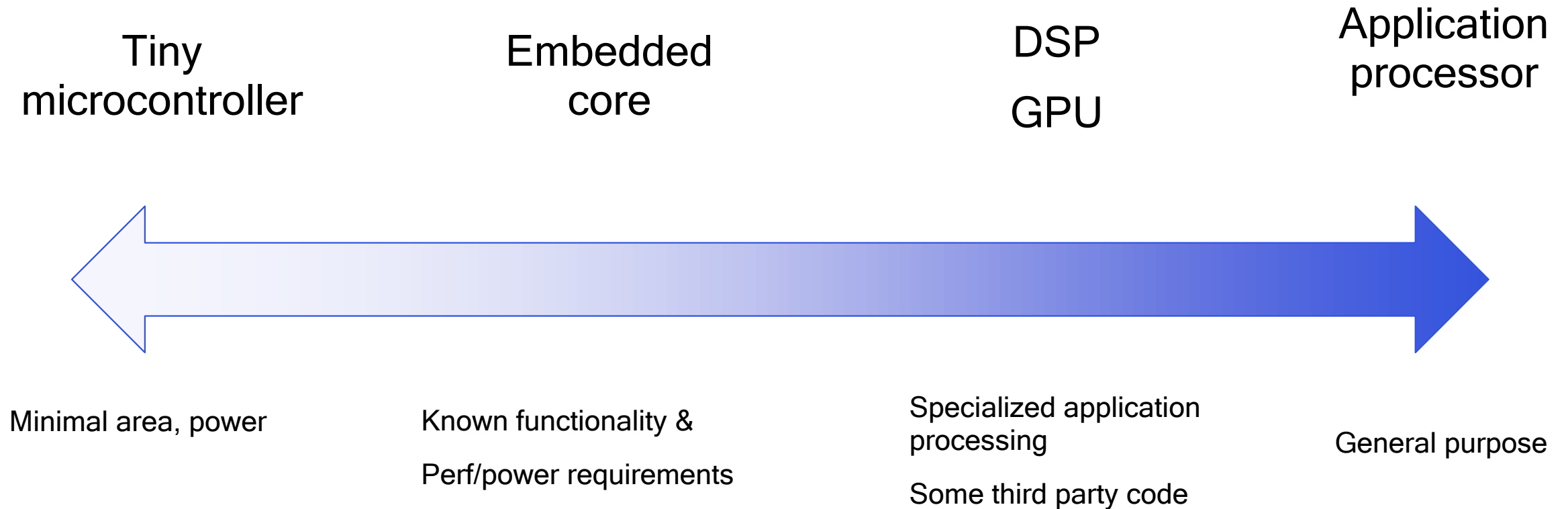GPS

Power mgmt

Wifi

PCIe
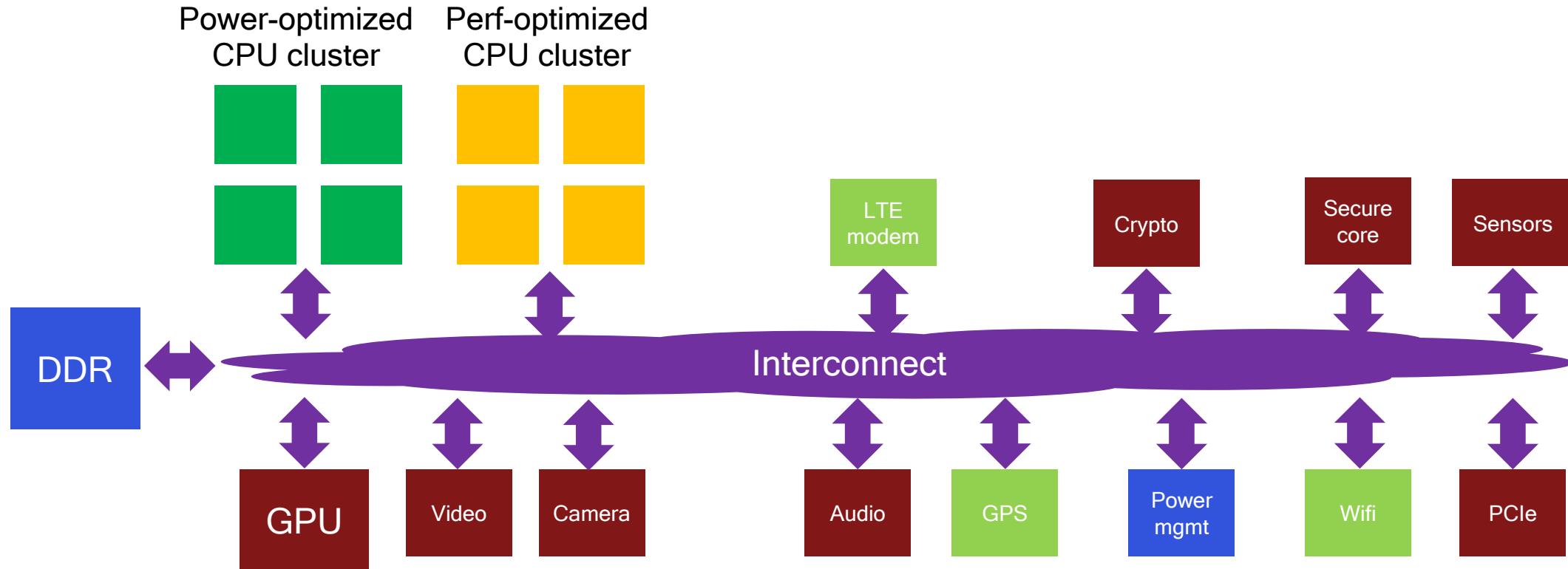
Complex system

- Multiple ISAs and software stacks

- Multiple roots of trust

- Multiple power domains

- Multiple product tiers and configurations

- Multiple development cycles across different components
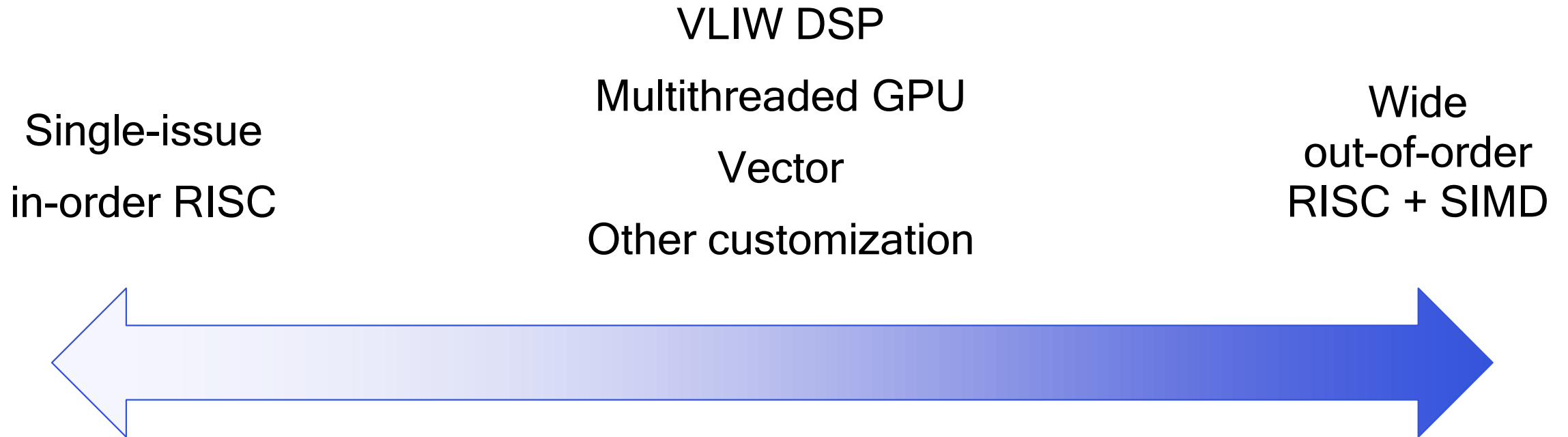
All across the spectrum

Scale of CPUs

Tiny
microcontroller

Embedded
core

DSP

GPU

Application
processor

Minimal area, power

Known functionality &

Perf/power requirements

Specialized application
processing

Some third party code

General purpose

Power envelope

"Always on"   ≈2 W

ISA & microarchitecture

VLIW DSP

Multithreaded GPU

Single-issue

in-order RISC

Vector

Wide
out-of-order
RISC + SIMD

Other customization

Software stack complexity

Lines of code – order of magnitude

100s

80 million*

* Not including 3rd party applications

ISA features and extensions

Customized for

- Signal processing

- Image processing

- Security

- Machine learning

- …

Minimal

High-level features

Multi-vendor standard

3rd party ecosystem

At least 6 different ISAs in use today in a single SoC

RISC-V: The opportunity
The power of freedom and open community

Customization

Mix-and-match extensions

Domain-specific features

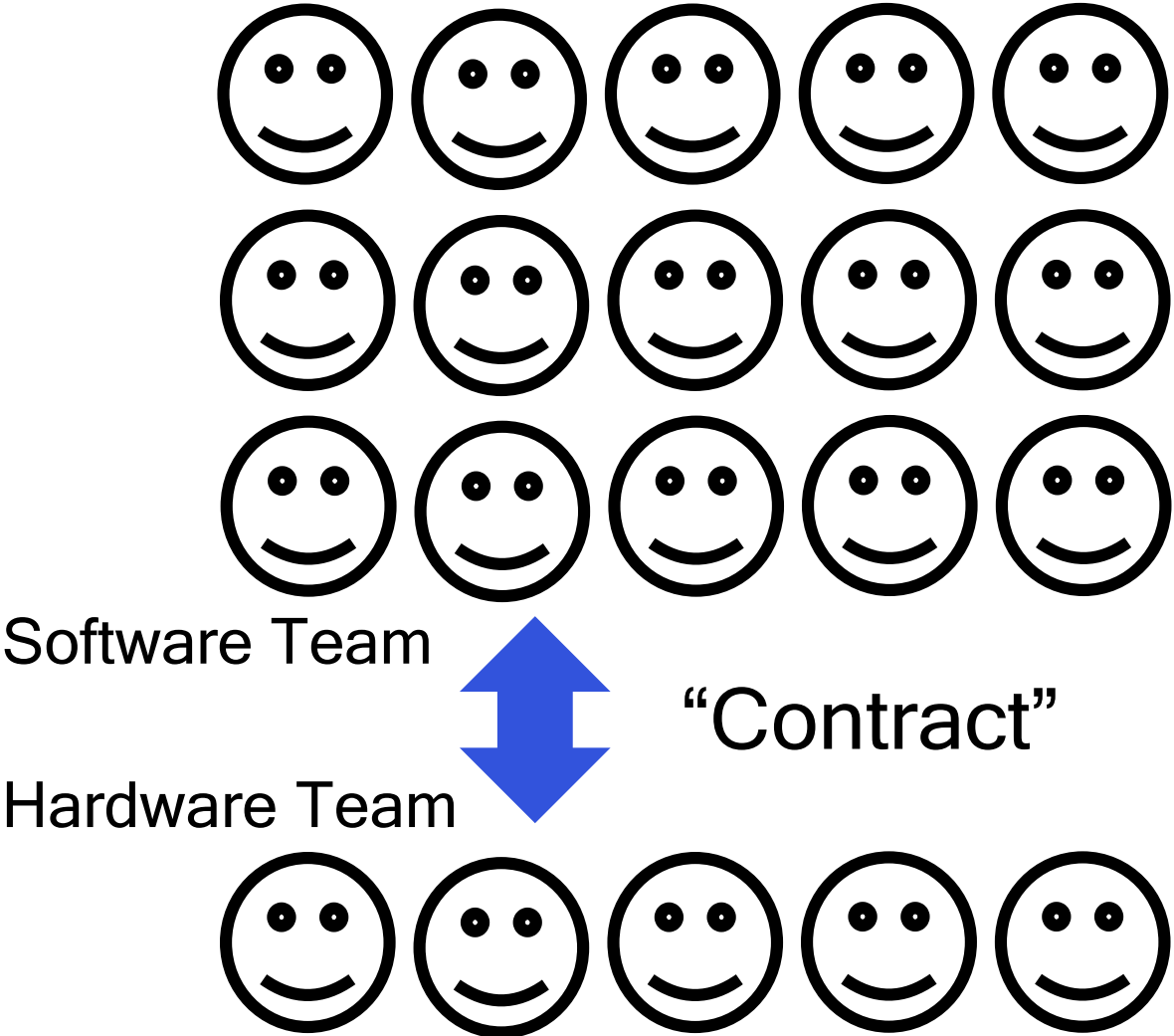Proprietary extensions ("secret sauce")
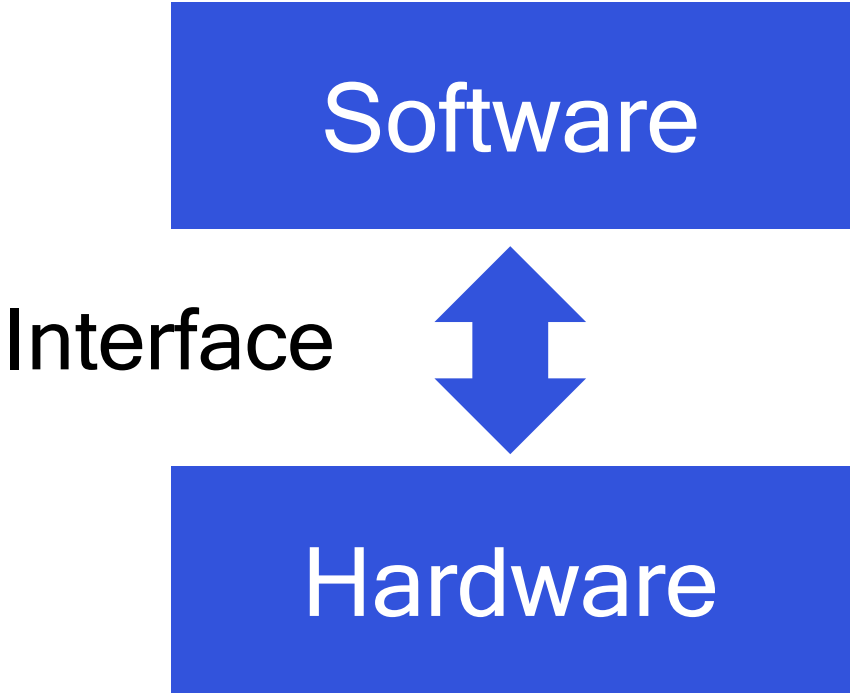
Spectrum of implementations (freedom to build)

+

Harmonization

Common base

Shared toolchains, infrastructure, libraries

Rich software ecosystem

What is ISA?

Two views

Software

Interface

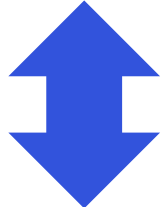Hardware

Software Team

Hardware Team

"Contract"

In practice
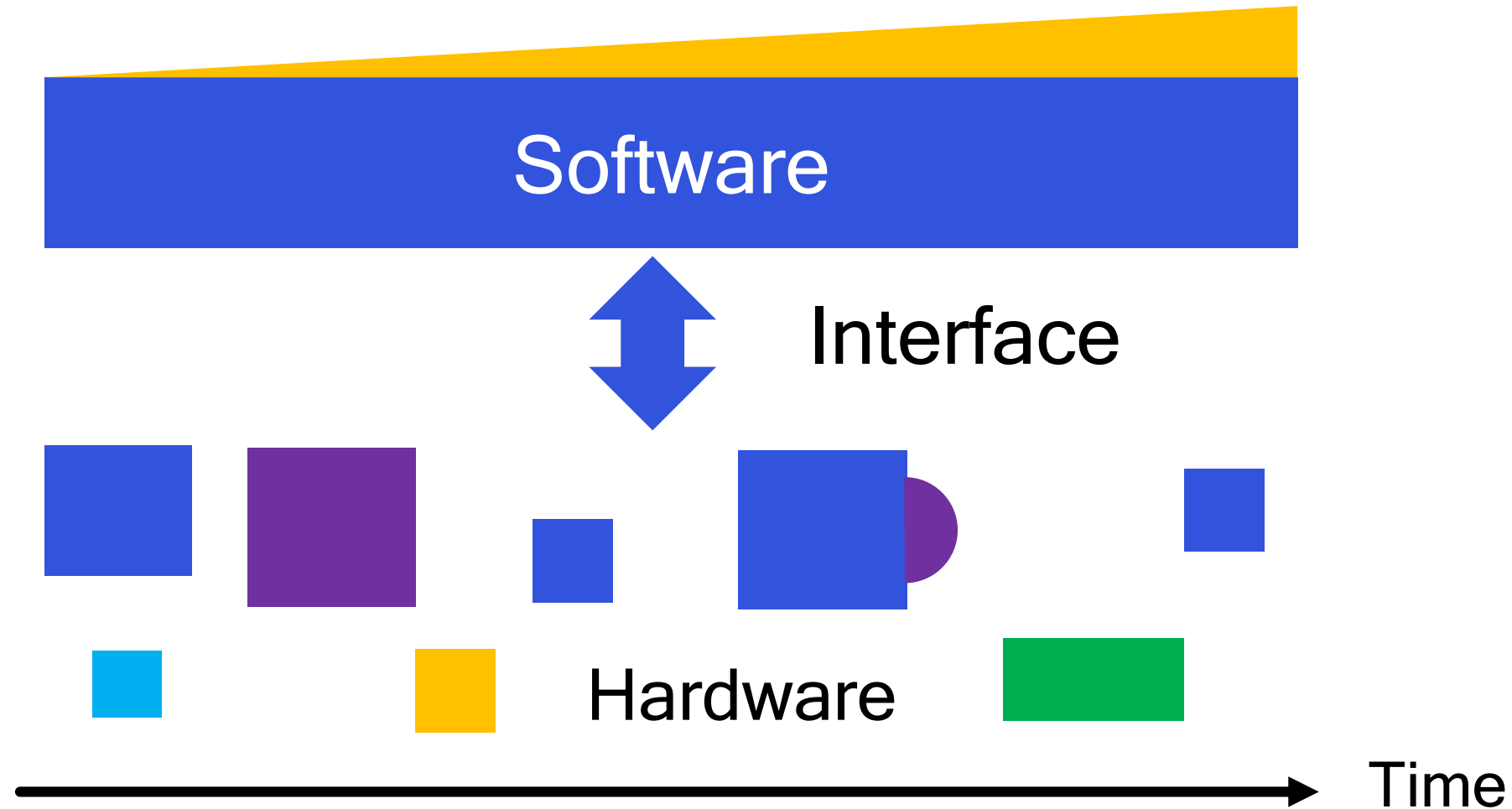
What is ISA?

My definition

Instruction Set Architecture, *noun*

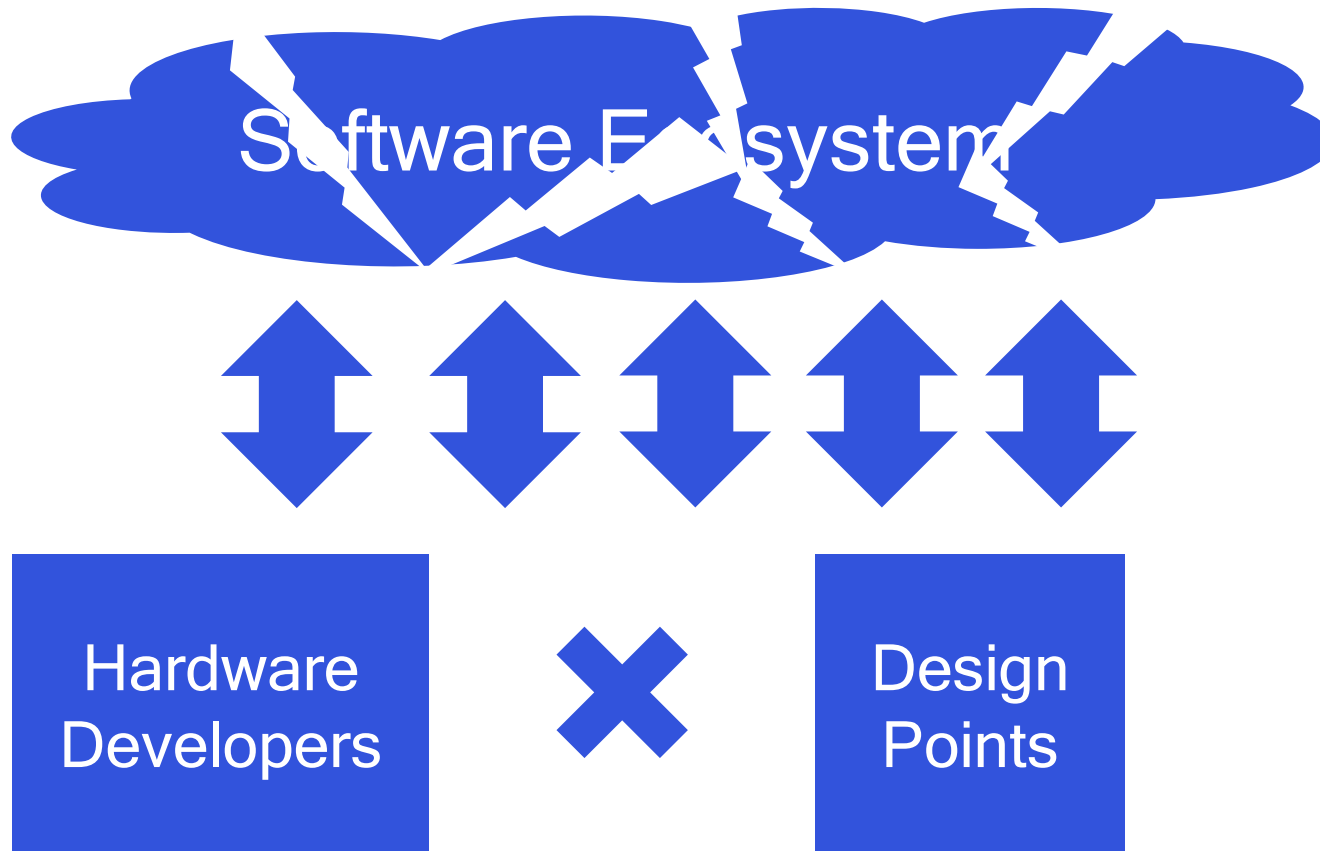The art of turning a hardware problem into a software problem

Software Ecosystem

Solutions

"Contract"

Hardware Developers ✕ Design Points

Means to an end

Software Ecosystem

Hardware Developers ✕ Design Points

"Multiple Contracts" ?

Changing over time?

RISC-V: The opportunity

The power of freedom and open community

Mix-and-match extensions

Customization

Domain-specific features

Proprietary extensions ("secret sauce")

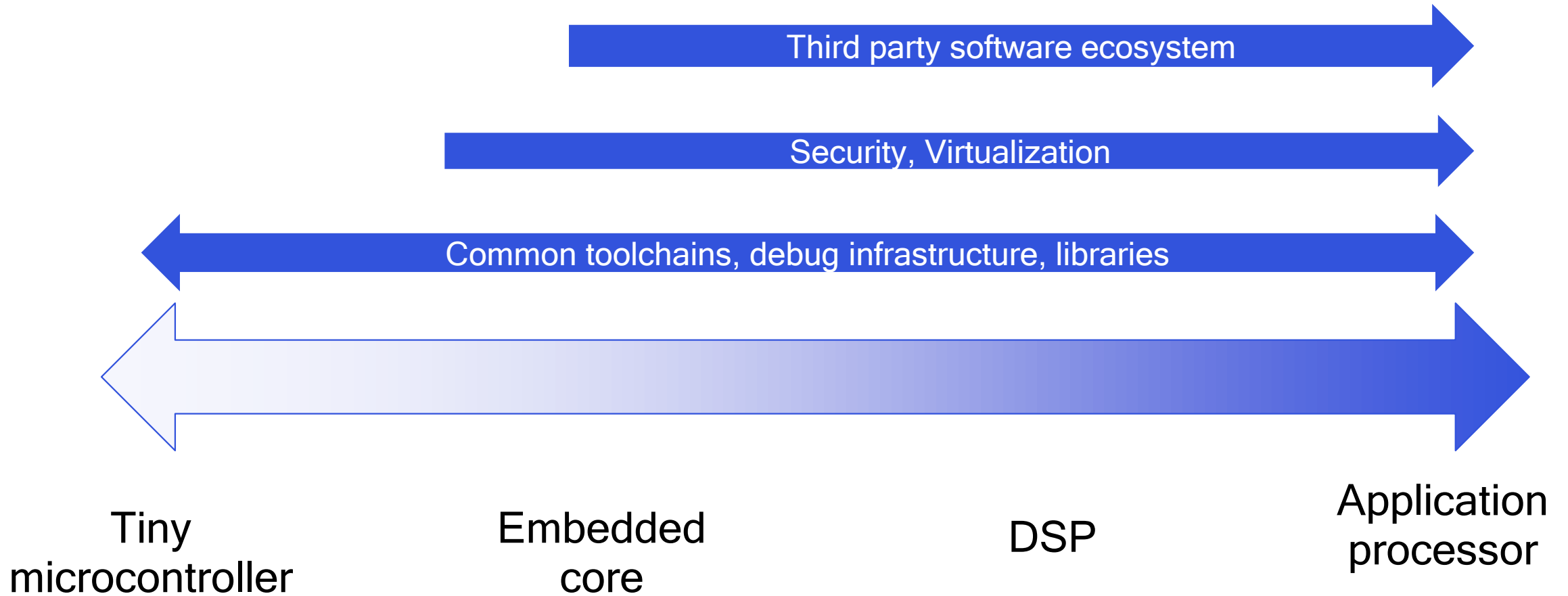Spectrum of implementations (freedom to build)

Tension

Harmonization

Common base

Shared toolchains, infrastructure, libraries

Rich software ecosystem

Core spectrum revisited

Minimize architectural tension

Third party software ecosystem

Security, Virtualization

Common toolchains, debug infrastructure, libraries

Tiny microcontroller

Embedded core

DSP

Application processor

RISC-V: The opportunity

- Great potential
  - Common base + ability to specialize where necessary
  - Enthusiastic community

- Opportunity to rationalize and simplify complex SoC design
  - Enable new features and capabilities

RISC-V: Some challenges

- Success = Attractive platform for solving problems
  - Software portability
    - Feature discoverability, not a unique software build per target
  - Interface stability vs evolution
  - Balancing hardware vs software needs

- Fragmentation is the enemy
  - Avoid a labyrinth of options, configurations, platforms
    - => Software and hardware test nightmare
  - Complex software needs standardization and stability
  - Good standards support a range of implementations *and* future evolution

Appeal to the community

- Come together, participate and standardize!
  - Bring experience & expertise => build the future on lessons of the past

- Lower-end and (future) high-end cores need to play nicely in a complex SoC environment:
  - Security
  - Virtualization
  - Memory models
  - Cache & TLB management
  - Power management
  - Interrupt delivery
  - Coexistence with current solutions (bus protocols, etc.)

Common platform

= reusable software

= growing ecosystem

- Great potential – let's make this happen!

An announcement

Qualcomm Technologies, Inc., will be shipping RISC-V in a high volume product in 2019

Qualcomm

Thank you!

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