

RISC-V Summit

DESIGN AND IMPLEMENTATION OF A RISC-V ISA-BASED IN- ORDER DUAL ISSUE SUPERSCALAR PROCESSOR

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**Ministry of Electronics and
Information Technology
Government of India**

Centre for Development of Advanced Computing



Design and Implementation of a RISC-V ISA based In-order Dual Issue Superscalar Processor

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C-DAC (Centre for Development of Advanced Computing)

C-DAC IS A premier R&D organization in IT&E (Information Technologies and Electronics) in the country working on strengthening national technological capabilities in the context of global developments in the field and responding to change in the market need in selected foundation areas. In that process, C-DAC represents a unique facet working in close junction with MeitY to realize nation's policy and pragmatic interventions and initiatives in Information Technology.

Processor Design Expertise

- ER902- 32- bit 5-stage pipeline RISC processor
- VAJRA64- 11-stage pipelined In-order Dual Issue Superscalar Processor
- ASHWA64 -Superscalar, variable-length, out-of-order pipeline

VAJRA64

- A 11-stage pipelined In-order Dual Issue Superscalar Processor based on RISC-V ISA based processor. VAJRA64 is designed for mid range embedded applications that require memory management unit for high level operating systems

Features

- ▣ Quad Fetch, In-order, Dual Issue, Superscalar Core
 - ▣ Support for 97 Instructions
 - ▣ 64 Bit Load Store Architecture
 - ▣ Pipelined Harvard Architecture
 - ▣ Byte, Half-Word ,Word and Double–Word Memory Access
 - ▣ Interrupt support
 - ▣ Multi-level MMU
 - ▣ Processor Modes-User, Supervisor and Machine
- I (Integer) - 55 Instructions
M (Mul/Div) - 13 Instructions
A (Atomic) - 22 Instructions
Privileged - 7 Instructions
RV64IMA

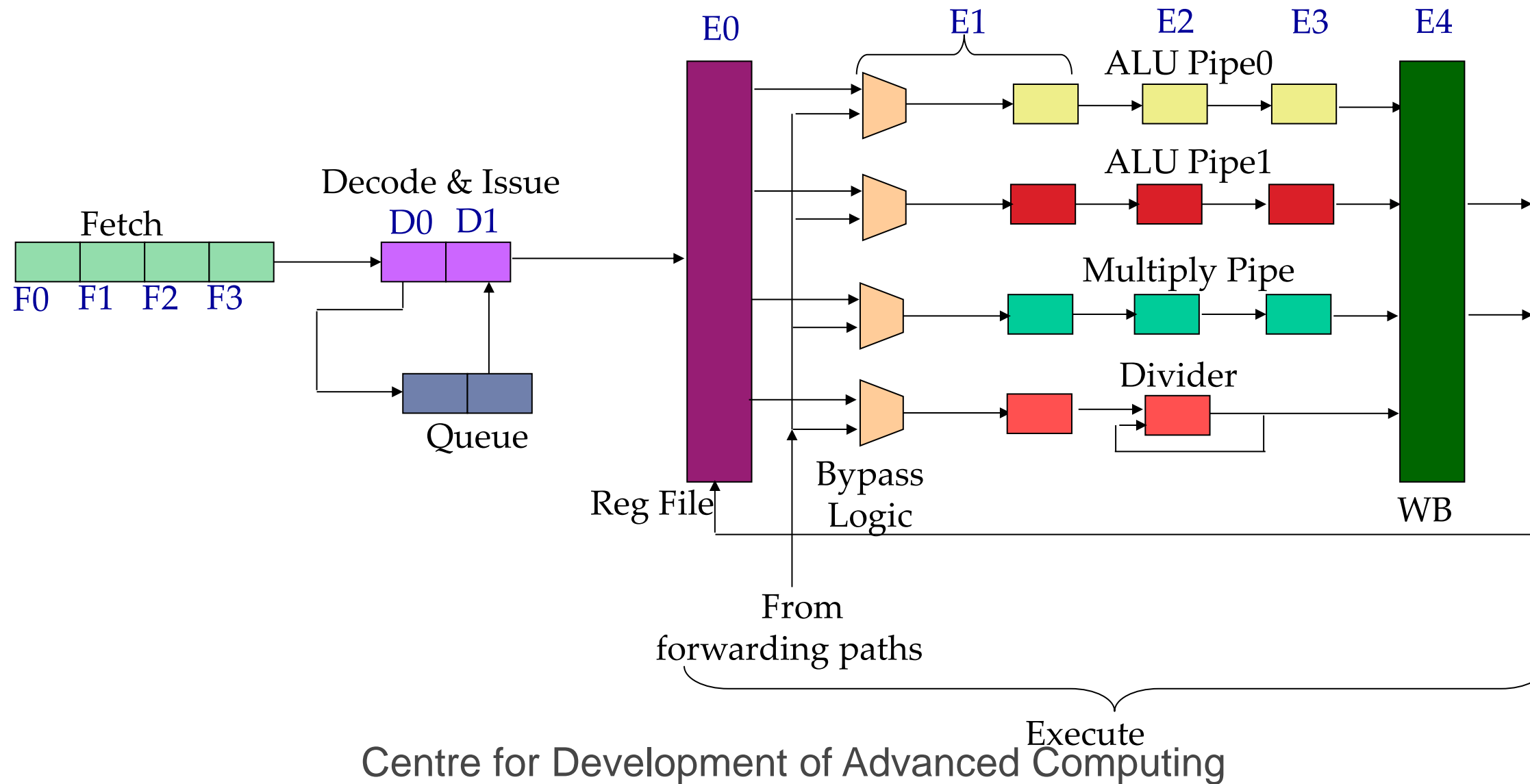
Features contd..

- ▣ RISC-V (RV64IMA) Instruction Set Architecture
 - User level ISA Version 2.0
 - Privileged Architecture Version 1.7
- ▣ 11 Stage Integer Pipeline
 - Fetch :: 4 Stage
 - Decode :: 2 Stage
 - Execute :: 5 Stage

Features contd..

- ▣ The four separate Execution pipes :
 - Asymmetric Integer lanes
 - Full ALU
 - Simple ALU
 - Multiply Lane
 - Divide Lane

VAJRA64 Architecture

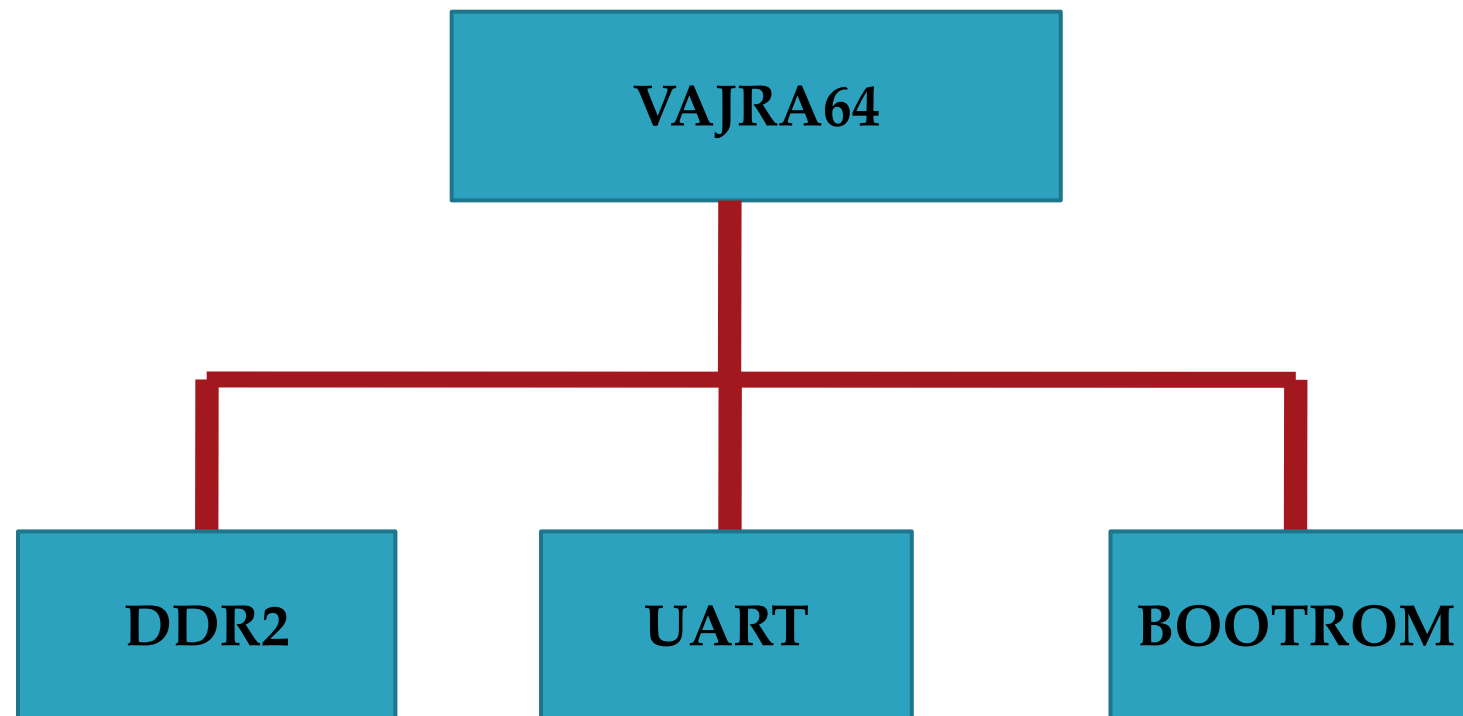


Synthesis results

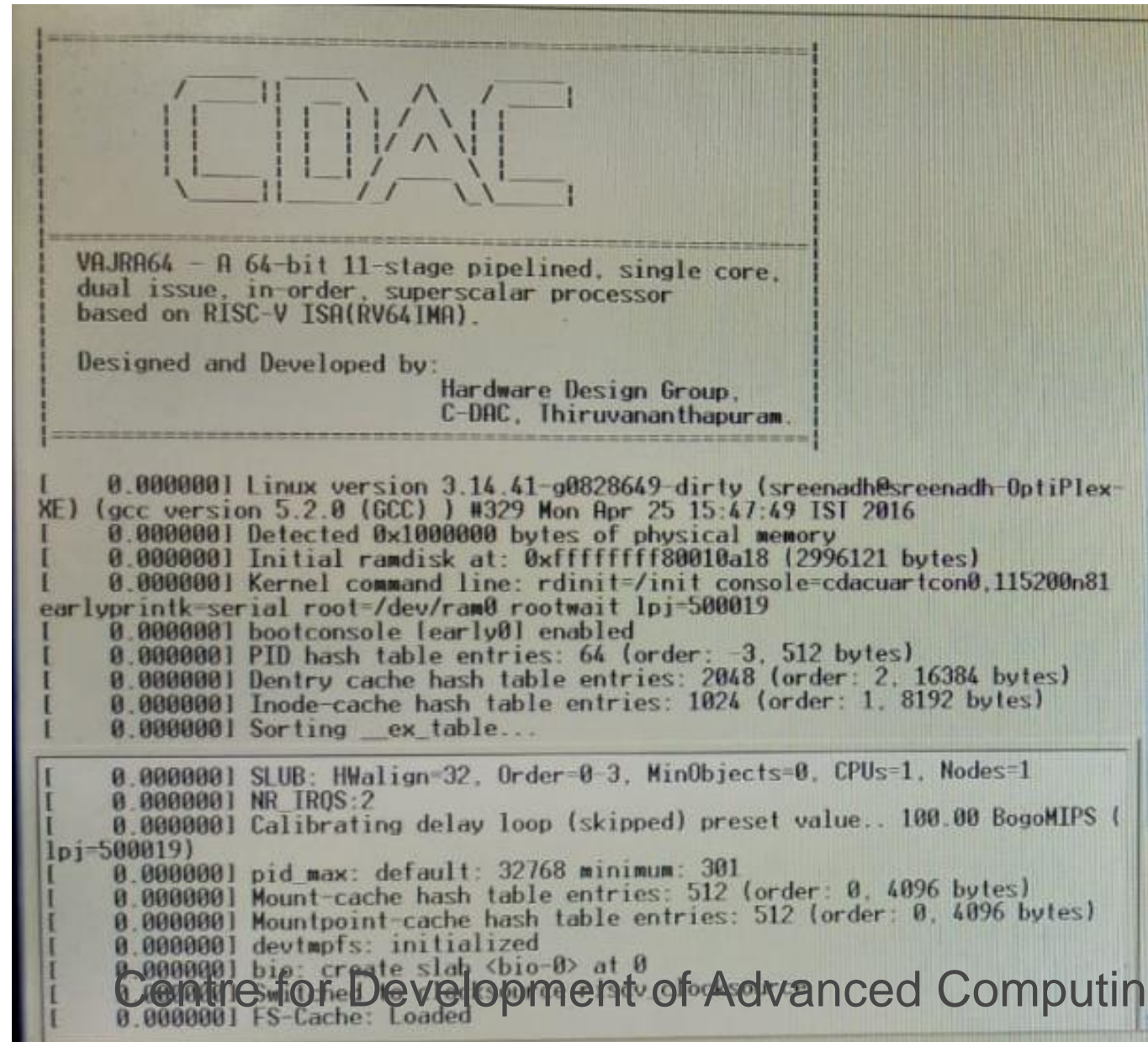
- Xilinx Kintex7 “xc7k325t-2-ffg900” FPGA.

Resource	
Slice Registers	48131
Slice LUTs	62517
LUT-FF pair	83043

Testing



Linux boot



```

[ 0.000000] Linux version 3.14.41-g0828649-dirty (sreenadh@sreenadh-OptiPlex-
XE) (gcc version 5.2.0 (GCC) ) #329 Mon Apr 25 15:47:49 IST 2016
[ 0.000000] Detected 0x1000000 bytes of physical memory
[ 0.000000] Initial ramdisk at: 0xffffffff80010a18 (2996121 bytes)
[ 0.000000] Kernel command line: rdinit=/init console=cdacuartcon0,115200n81
earlyprintk=serial root=/dev/ram0 rootwait lpj=500019
[ 0.000000] bootconsole [early0] enabled
[ 0.000000] PID hash table entries: 64 (order: -3, 512 bytes)
[ 0.000000] Dentry cache hash table entries: 2048 (order: 2, 16384 bytes)
[ 0.000000] Inode-cache hash table entries: 1024 (order: 1, 8192 bytes)
[ 0.000000] Sorting __ex_table...

[ 0.000000] SLUB: HWalign=32, Order=0-3, MinObjects=0, CPUs=1, Nodes=1
[ 0.000000] NR_IRQS:2
[ 0.000000] Calibrating delay loop (skipped) preset value.. 100.00 BogoMIPS (
lpj=500019)
[ 0.000000] pid_max: default: 32768 minimum: 301
[ 0.000000] Mount-cache hash table entries: 512 (order: 0, 4096 bytes)
[ 0.000000] Mountpoint-cache hash table entries: 512 (order: 0, 4096 bytes)
[ 0.000000] devtmpfs: initialized
[ 0.000000] bio: create slab <bio-0> at 0
[ 0.000000] FS-Cache: Loaded

```

Targeted applications

- ▣ Consumer devices
- ▣ Home networking appliances
- ▣ Embedded computing
- ▣ Printers
- ▣ Strategic

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THANK YOU

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