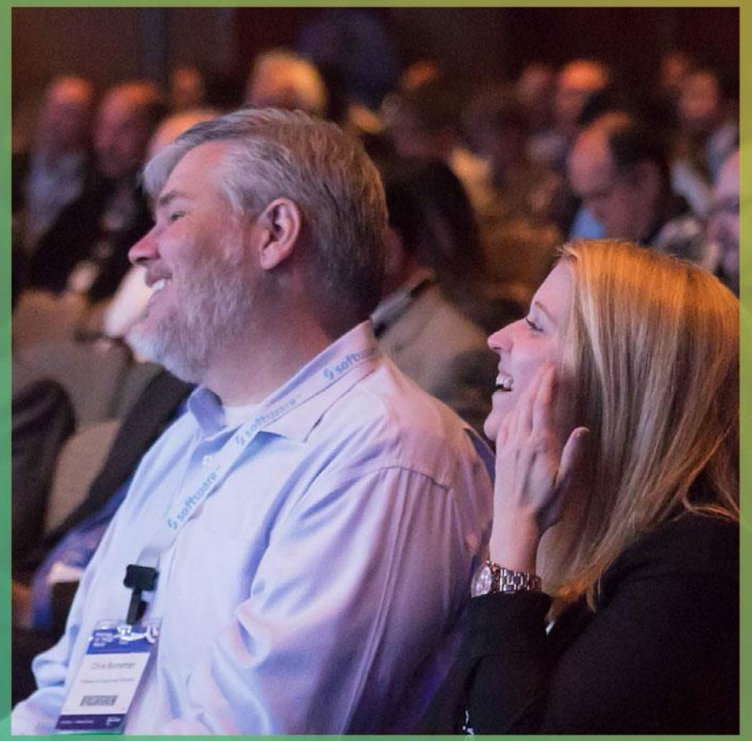
RISC-V Summit

December 3 - 6, 2018
Santa Clara Convention Center
CA, USA



REVOLUTIONIZING THE COMPUTING LANDSCAPE AND BEYOND.

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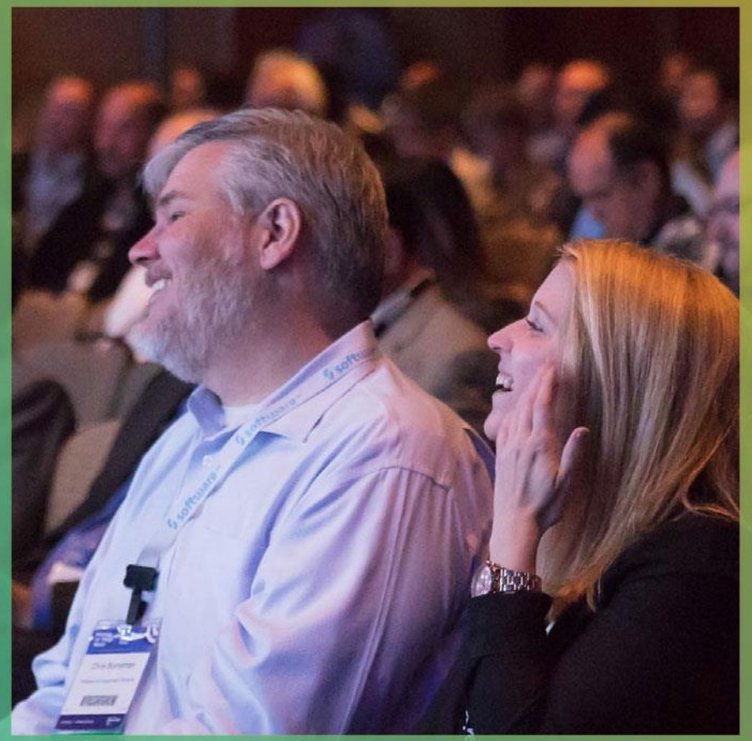
RISC-V Summit

MASSIVELY PARALLEL RISC-V PROCESSING WITH TRANSACTIONAL MEMORY



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Introduction

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- Discuss Transaction Memories
- Walk Through an Example Implementation, Utilizing Transactional Memories and RISC-V Harts
  - Full Chip, Island, Cluster and Groups of RISC-V Harts
- RISC-V Feature Set for RFPC
- Summary

“Transactional Memory”

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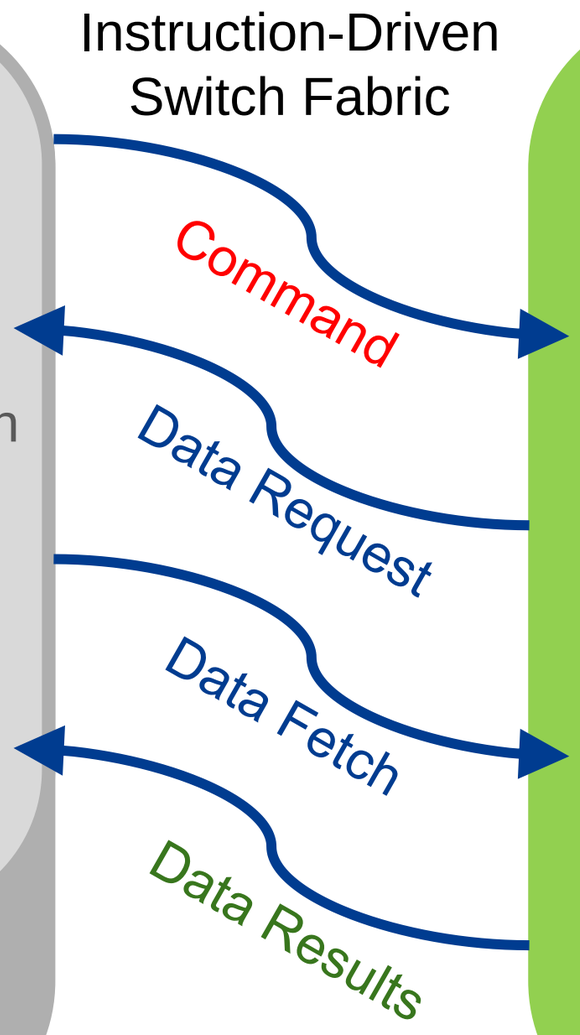
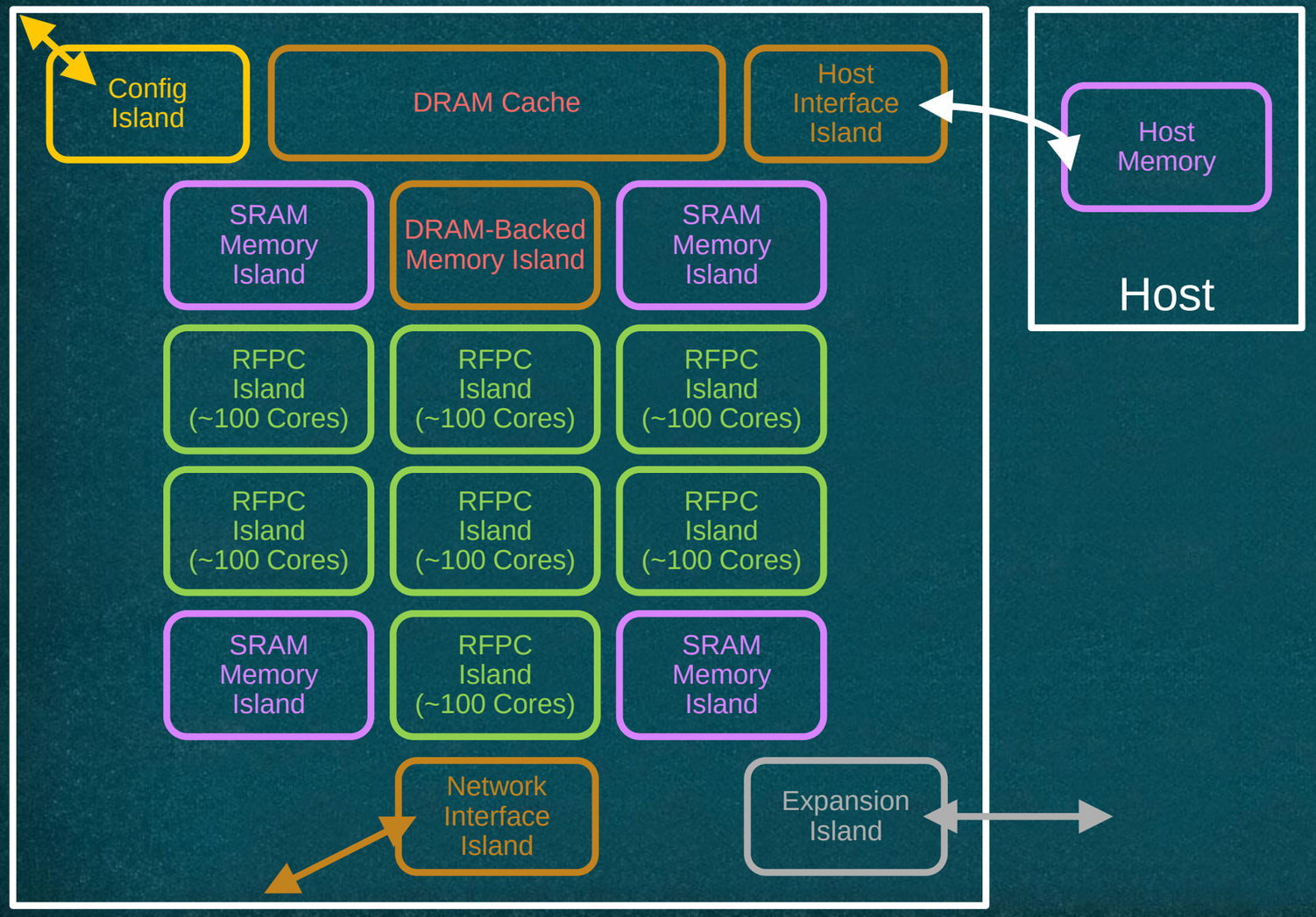
- Many, Many CPU Cores
- Require
  - Many Cores
  - Efficient Command Dispatch / Fetch / Result / Synchronization
- (Not interrupt based for example…)!
  - WFE
  - Currently Planned as Custom-1

But still running in arbitrary C code of any size ...



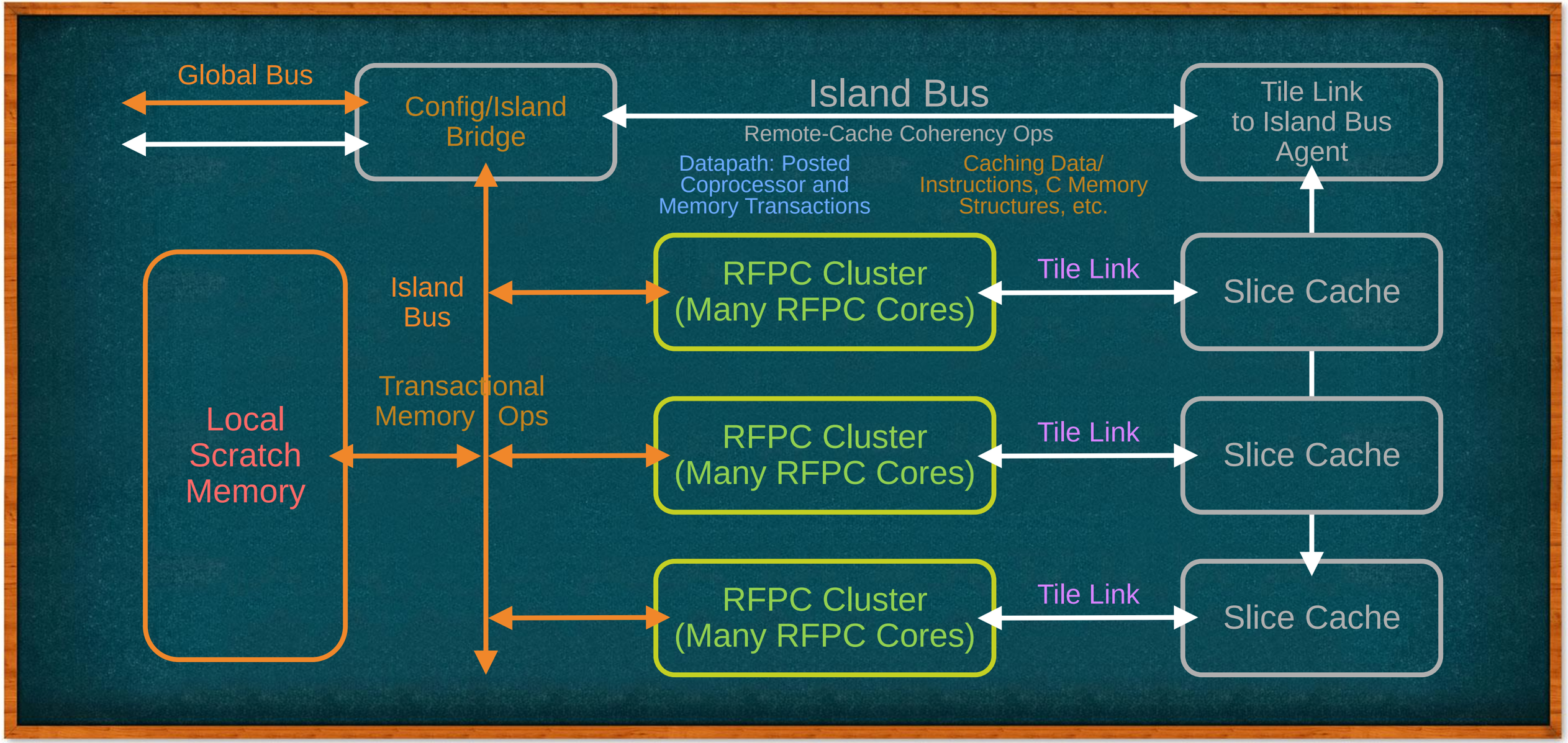
- Transactional Memory Hierarchy
  - Memory
  - Closely coupled
    - Threaded processing engines
    - And hardwired transaction types
      - Atomics
      - CRC
      - Crypto

A Practical Implementation

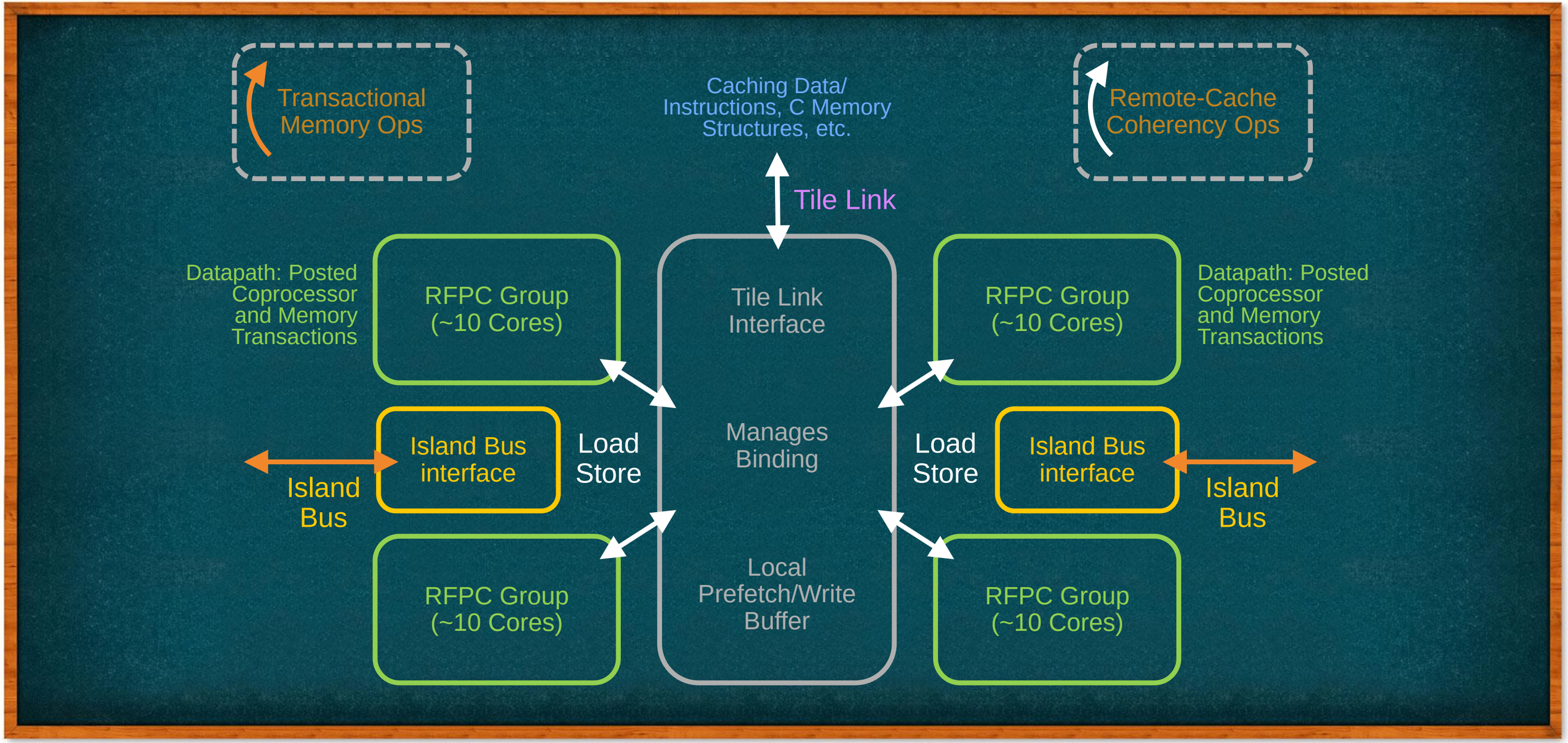


- The chip or chiplet is made up of islands, which are connected through the instruction-driven switch fabric
- Which allows for implement-tation from small to large
- Memory hierarchy provides equal access to all types of memories
- The config, host interface, and network interface islands allow for feeding data into the system
- Basic flow of data in a SmartNIC

RFPC Island



RFPC Cluster



RFPC Group

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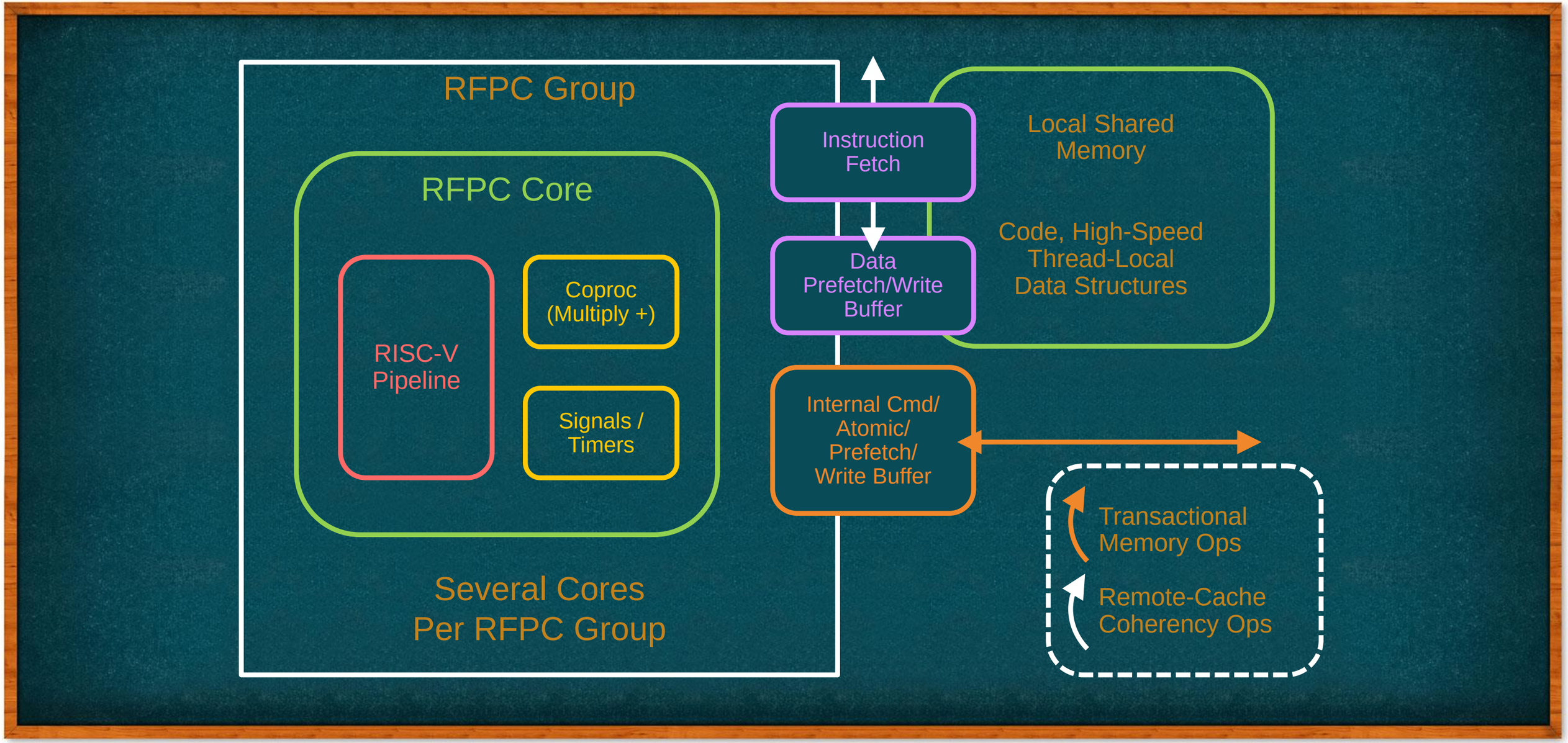

RISC-V Feature Set for RFPC

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RFPC Cores are RV32IMC cores with custom-0/1 instructions

RV32IMC keeps the performance high with low silicon gate count; support for User, Machine and Debug modes only, but provides some memory protection and both user-level and machine-level interrupts.

Custom-0 instructions permit dynamic binding of 48+-bit host address and bulk DDR addresses to 32-bit RISC-V addresses

Custom-1 instructions permit transaction memory and signaling operations

RFPC Cores collected into RFPC groups

Sharing local memory, which is directly accessed (not cache)

Simple address translation permits core-local data and stack without changing code and register initialization values

RFPC Groups collected into RFPC Clusters

Transaction initiation and signal handling (for transaction acceptance/completion) are handled also in the island bus interfaces.

Island bus access through a shared memory, and local transactional (atomic pipeline) memory shared within the cluster only. Non-transactional access to the cache slices

RFPC Clusters collected together

RISC-V Debug module shared amongst 40 cores - permits JTAG-based debugging of every core

The slices of cache combine as ‘L2’ cache

Provides windowing to 48-bit PCIe and 40-bit MU address spaces

RFPC is size and performance optimized

Summary

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- RISC-V harts are well suited for the processor required for implementing a thousand CPU Smart-NIC.
  - The RISC-V solutions can be tailored to meet the needs for embedded applications with suitable choice of instruction set features, privileged modes and debug methodology.
  - We covered at a high level the organization of memories and RISC-V harts that provides efficient processing with high latency memory transactions
  - We looked at the instruction set customizations that allow this to handle RISC-V hart interaction with the memory systems and other harts

ODSA Workgroup

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Implementing open specifications contributed by participating companies, any vendor's silicon die can become a building block that can be utilized in a chiplet-based SoC design

Working together to standardize processors, accelerators, and memory and I/O peripherals using optimal process nodes

Companies wishing to learn more, participate and become an integral part of the ODSA Workgroup can inquire further at odsa@netronome.com or visit us in **booth #407**!

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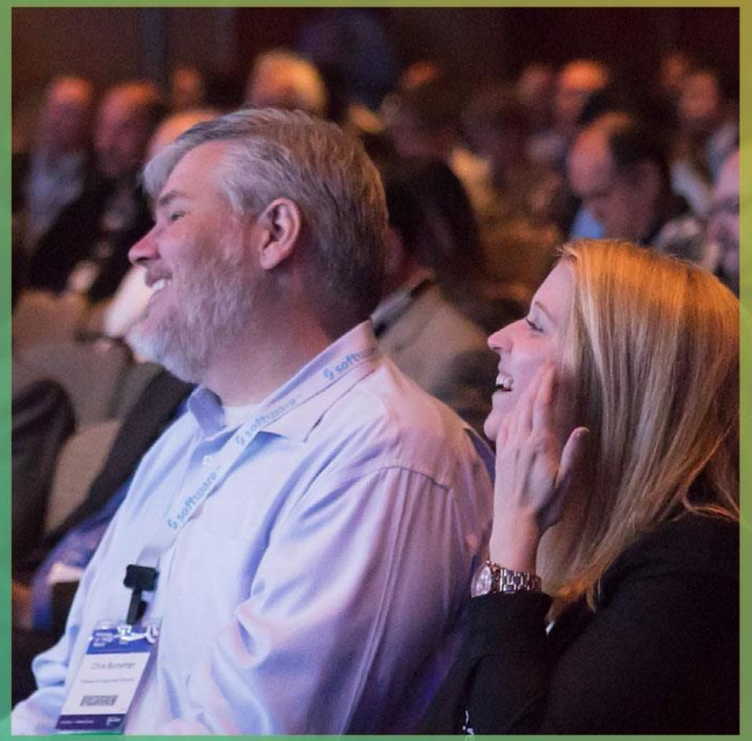
THANK YOU



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