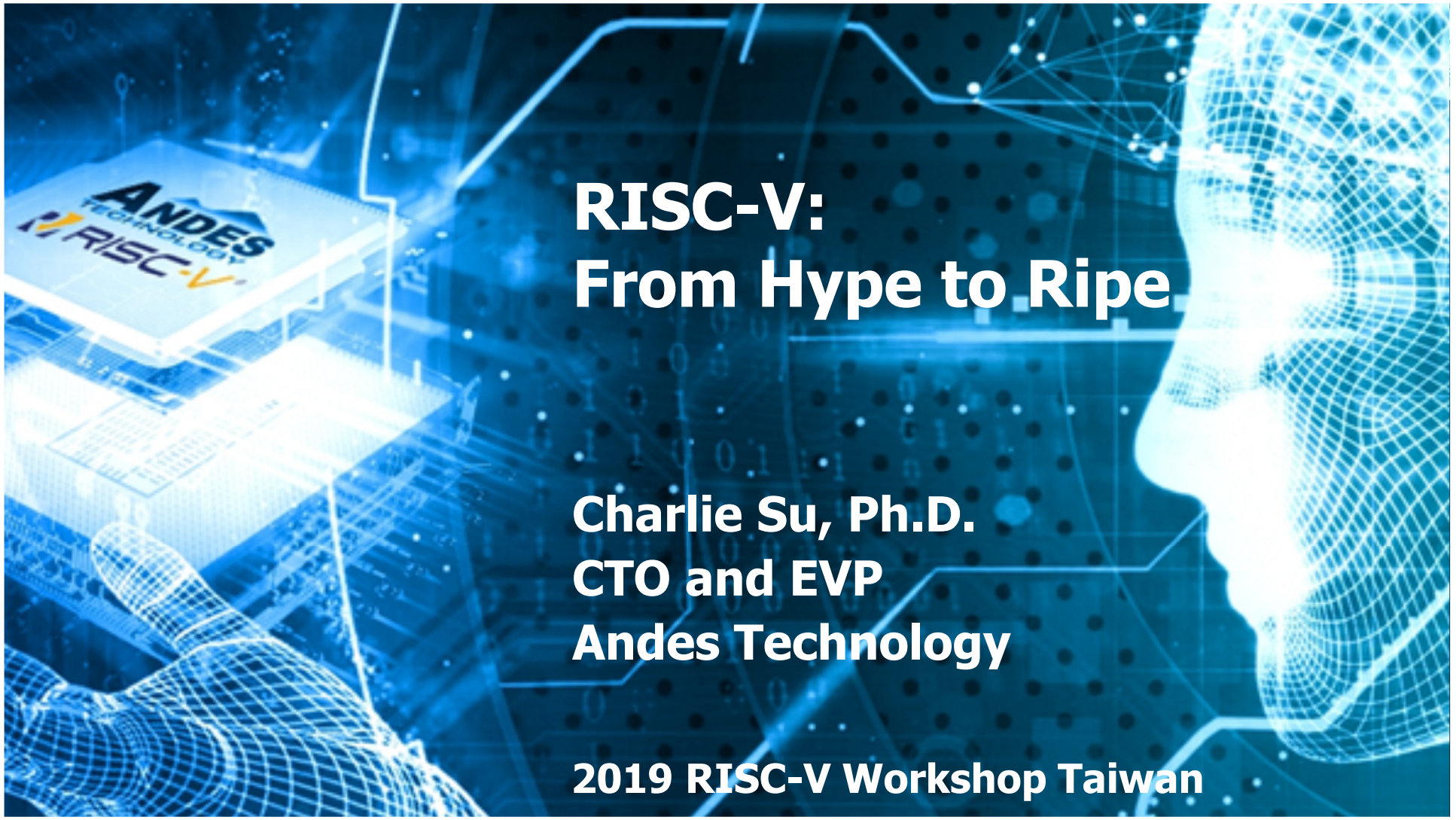


RISC-V: From Hype to Ripe

Charlie Su, Ph.D.
CTO and EVP
Andes Technology

2019 RISC-V Workshop Taiwan

From Hype to Ripe

- Like "different" in "Think different"
- "Ripe" is used as a noun
  - readiness for harvest
  - readiness for action

- RISC-V starts with hype
- But, those involved early are ripe in diversified applications

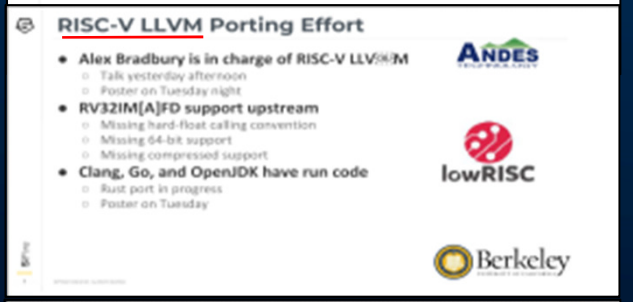
Overview of the Talk

- A Fast Advancing Architecture
- Hype and Expectation
- Some Challenges and Andes Approaches
- Concluding Remarks

Andes Technology Corporation

- A 14-year-old public CPU IP company
- >150 licensees worldwide
- >1B Andes-Embedded SoC shipped in 2018

- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involved in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) TG
  - Co-chair of Fast Interrupt TG
  - Preparing the Performance Tools TG



RISC-V: A Fast Advancing Architecture

- **Open and free ISA from Berkeley to the Foundation**
- **200+ members include leaders from all fields**
- **RISC-V as an open standard**
- **Technical merits of RISC-V**
  - Clean-Slate
  - Compact: small kernel (I/E)
  - Modular: M, A, C, F, D
  - Extensible: reserved space for vendor's innovations
- **More RISC-V specs continue to advance**
  - ISA: B, J, P, S, V
  - Privileged spec and debug spec
  - Fast Interrupts, Memory Model, Trace

➔ Any good ISA (or any standard) should always move forward

Hype and Expectation

- **Hype and expectation**
  - Isn't RISC-V Free? Can I have your RTL? Why do you charge this and that?
  - RISC-V is very hot. So, it must get everything and I want a core with XYZ.
- **Confusion and concern**
  - Some worry that extensions lead to fragmentation
  - But, they ask for their specific features
- **Where does the hype come from?**
  - Results of how we promote RISC-V
    - "Free" is confusing. "Open" seems to work better.
  - Mostly, information asymmetry due to fast advancing of RISC-V
- **Hype isn't necessary bad. It gets massive attention**
  - We just need to work hard to meet/beat the expectation

Challenge – Business Models

- **Large membership of RISC-V Foundation**
  - It's OK to have healthy coopetition
  - More importantly, create competitive edge over other architectures
- **Many open source RISC-V cores out there**
  - Good in getting people interested in and evaluating RISC-V technologies
- **Free or cheap often most expensive**
  - Plenty of free cores in the past: DLX from the book, OpenRISC, etc.
  - Serious design teams choose "**RISK-FREE**" over "**FREE RISC**"
- **Between very expensive and free/very cheap**
  - Room for sustainable business models to help customers and grow RISC-V

Innovate Cooperation

- **Cooperate tightly to advance RISC-V faster**
- **RISC-V EasyStart program:**
  - Motivation: Many companies don't design/implement their chips
  - Andes works with **15 Design Service partners** to help those companies to adopt RISC-V easier
- **Product development:**
  - Andes partners with **Nuclei** to develop AndesCore 22-series for our common market
- **Welcome new ideas**

Challenge – Spec

- **Development cycle**
  - Solid spec deserves time investment to finalize
  - But, business opportunities often demand something sooner
- **Clean slate vs. legacies/existing practices**
  - A clean slate is elegant and easier to implement
  - But, there are legacies and existing practices
  - Examples:
    - Everything is cacheable and coherent in RISC-V
      - Uncached usage does exist
      - Simple systems manage caches by SW
    - No place to specify cacheability policy (writeback, write-thru, etc.)
      - Sometimes, write-thru is needed along with writeback

V5: Best Extensions to RISC-V

AndeStar™ V5: RISC-V + Andes Extensions

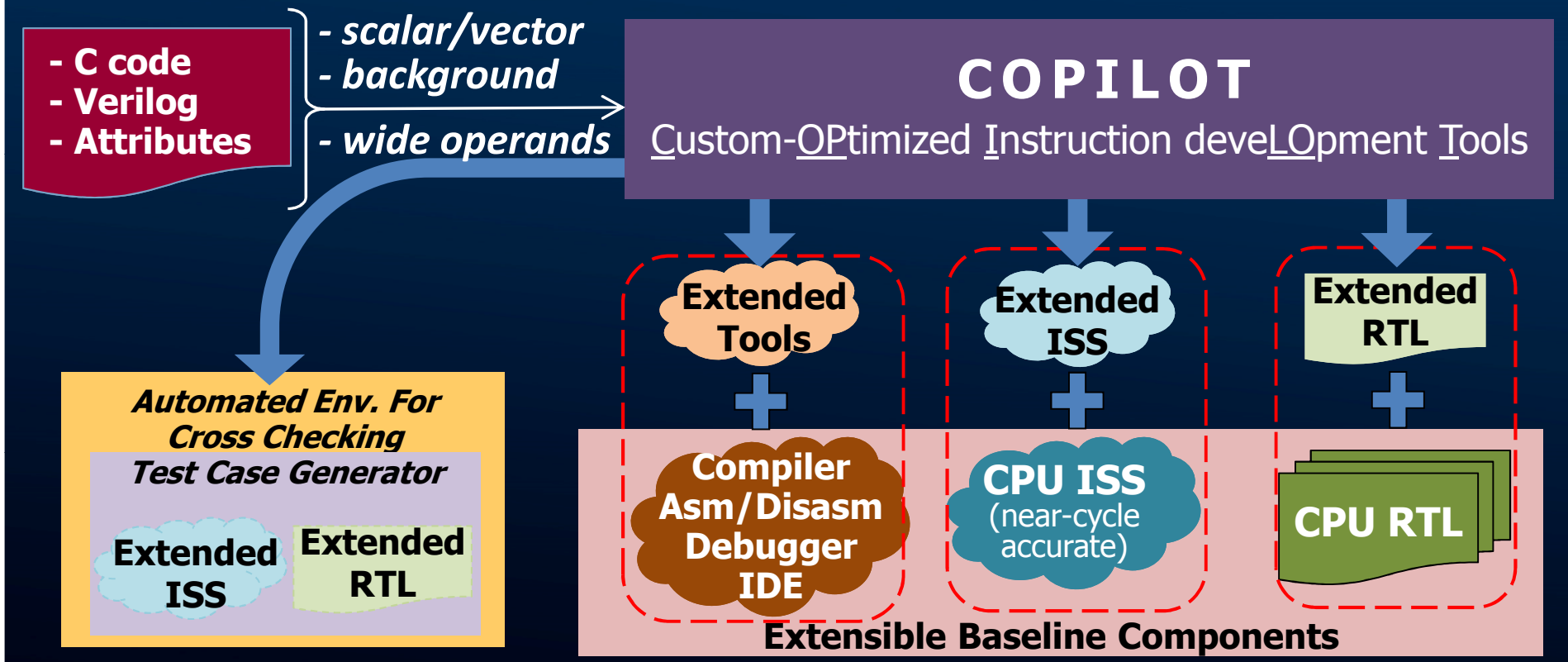
- **Fully support the standard**
- **Custom Extension is key to advance RISC-V**
  - Serve broader market
  - Make RISC-V even more competitive when needed
  - Innovate DSA in respective target markets
- **Vector interrupt controller with priority-based preemption**
- **Comprehensive cache features**
- **Point features:**
  - StackSafe™, QuickNap™, PowerBrake
- **Baseline ISA extensions**
- **Andes Custom Extensions™ (ACE)**

Krste Asanovic[1], Healthy Discussion of Architectural Choices[2]:

RISC-V was designed to **support specialization** while avoiding fragmentation by **mandating a frozen common ISA standard** around which the software community coalesces, while leaving ample space for **innovative custom extensions** that do not interfere

1: Chairman of RISC-V Foundation, Berkeley Professor, and SiFive co-founder
2: EE Times, 7/11/2018

Andes Custom Extension™ For DSA



Example: Madd32

madd32.ace

```
insn madd32 {
   operand= {io gpr acc,
             in gpr data, in gpr coef};
   csim= %{
      acc+=(data & 0xffff)* (coef & 0xffff)
          + (data >>16)    * (coef >>16);
   %};
   latency= 1;
};
```

madd32.v

```
//ACE_BEGIN: madd32
  assign acc_out = acc_in
         + data[15:0] * coef[15:0]
         + data[31:16]* coef[31:16];
//ACE_END
```

ACE vs. coprocessor signals: C/C++ vs. Assembly

Challenge – Fragmentation

- **People are alert to the potential fragmentation due to extensibility**
- **How many possible combinations from the standard IE-MCFD?**
  - 10 from I-MCFD: I, IM, IC, IMC, IMF, IMFD, ICF, ICFD, IMCF, IMCFD
  - Another 10 from E-MCFD (from 32 to 16 GPRs)
  - Additional 12 from the newly-proposed Zfinx (putting FP in GPR)
  - Get even more interesting with B/J/P/S/V
- **Extensions, standard and custom, could lead to fragmentation**
  - If not managed well.
  - But, this has been well-handled before in other architectures
- **How Andes managed V1/V2/V3 + F/D + DSP**
  - HW contains information indicating its capability (RISC-V has Device Tree)
  - ELF files contain HW capabilities used and loader does the check
  - IDE simplifies user's selection/setting in toolchains

Concluding Remarks

- **JFK, the father of open source:**
  - Don't ask what the community can do for you
  - Ask what you can do for the community
- **Community is a great force to advance technologies**
  - But, you must be able to work with it and tolerate its pace

Concluding Remarks

- **RISC-V started with hype**
  - But followed with healthy and fast-paced standard advancement
- **It's ripe for the emerging opportunities**
  - and pretty much for all computing devices
- **Andes for those needing professional RISC-V cores**
  - A pure-play processor IP vendor for RISC-V
  - Trusted Computing Expert already helped shipping billions of SoC
  - Working with many partners to serve the market
  - Diversified applications:
    - AI, 5G, FPGA, IoT, MCU, Security, Storage, Wireless
- **Come join RISC-V**

See What Andes Has Been Driving

Tuesday:

Chuanhua Chang, 11:20
Status update of RISC-V P extension task group

Charlie Su, 13:45
New Members of AndeStar V5 Processor IP's

Wednesday:

Kito Cheng and Greentime Hu, 9:35
The updated status of RISC-V SW

Alan Kao, 10:05
RISC-V Perf Tool Status

Shiva Chen and Hsiangkai Wang, 11:15
Compiler support for linker relaxation

Tuesday:

NTU (Zhen Wei), 11:35, Simulation Evaluation of Chaining Implementation for the RISC-V Vector Extension

NCTU (Chien-Hao Chen and Po Yu Huang), 16:05, Energy-Efficient Face Detection Using Andes RISC-V Processor

NTHU (Allen Lu and Prof. JK Lee), 16:45, Enabling TVM on RISC-V Architectures with SIMD Instructions

NTU (Wen-Cong Huang and Chia-Hsiang Yang**), Poster, 17:10,** RISC-V Architecture Optimization through Extensible Instruction Sets and Custom Accelerators

Thank You !!