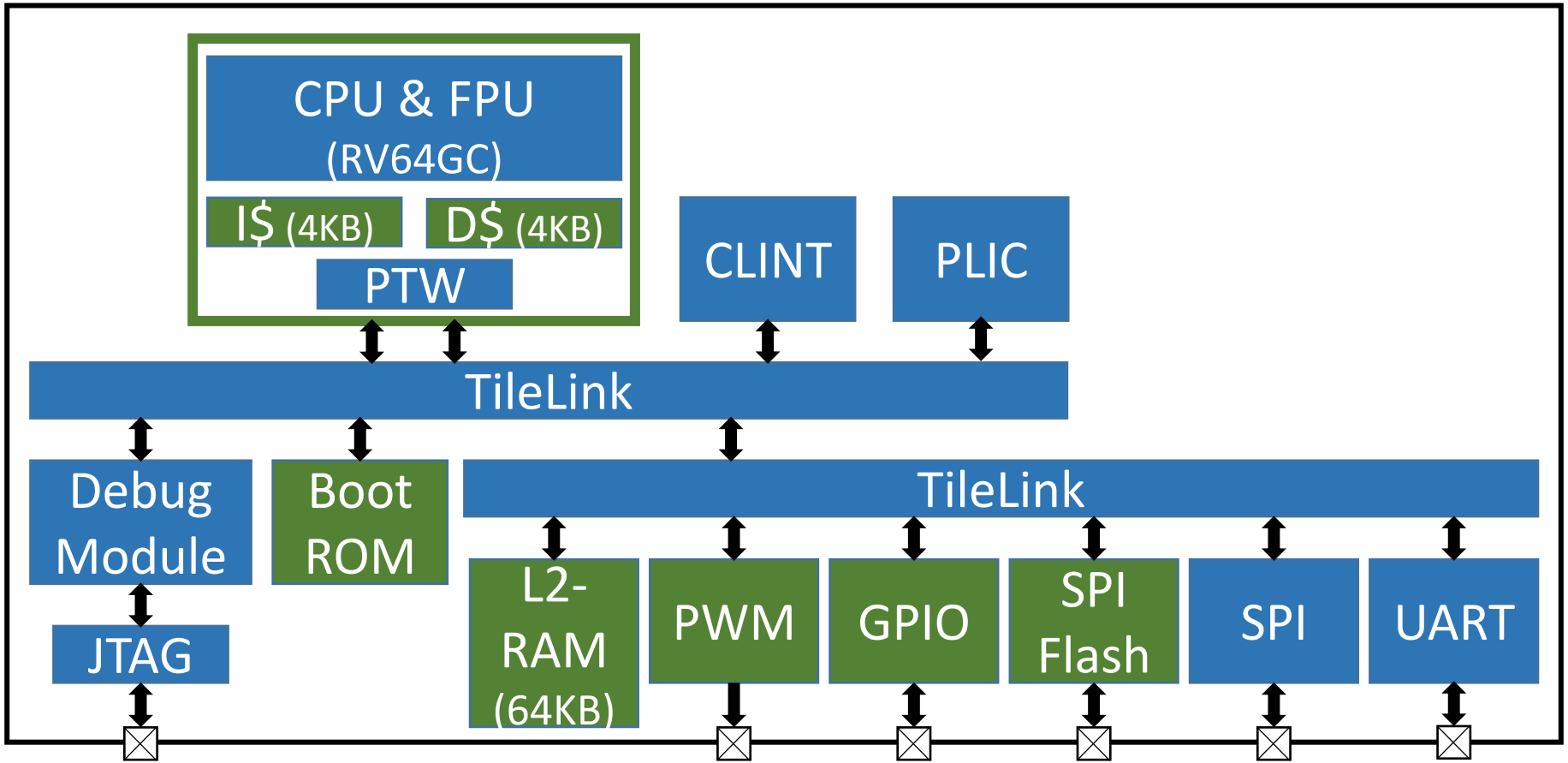
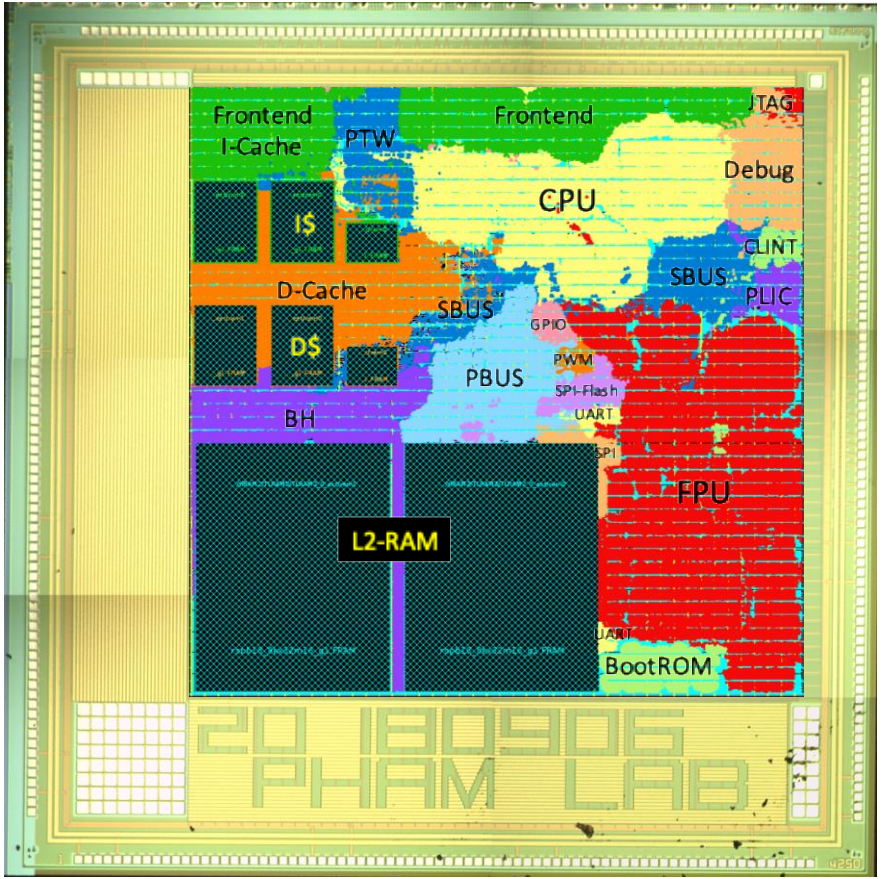
64-bit RISC-V Chip with MMU, L1 and L2 Memories



Implementation Result



Process: 0.18um (ROHM)
Area: 3.75mm x 3.75mm
SRAM:
I$ + D$: 4KiB + 4KiB
L2-RAM: 64KiB
Std. Cell: 302KG (Utilization: 53%)
Voltage: 1.8V
Frequency: 80MHz @typ (not optimized)

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