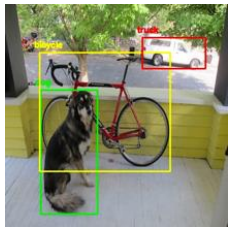
Overview

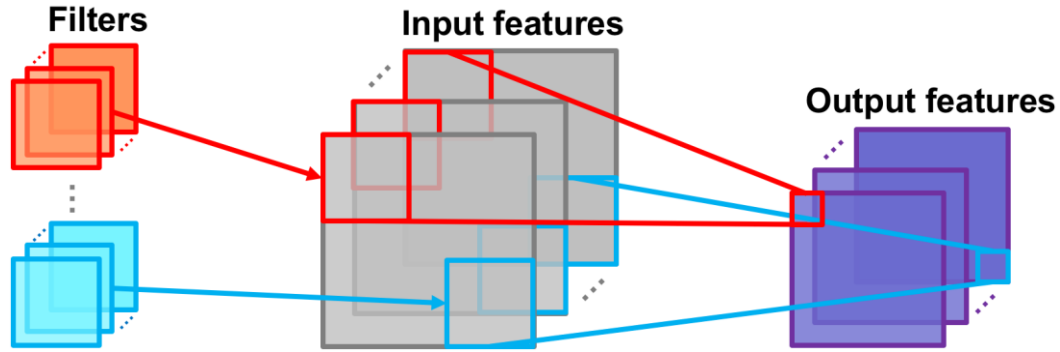
- **Applying RISC-V core with custom instructions to mobile AI**

recognition



detection

segmentation



Conv layers: >90% computation in CNNs

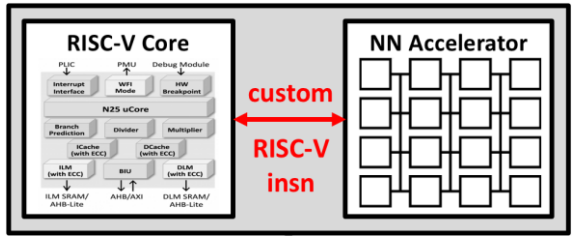
- **Profiling RISC-V program with additional custom instructions**
- **Evaluating hardware performance for multiple configurations**

```
insn crc32 {
  op = {out gpr crc, in gpr data};
  csim = %{
    char           dat8b[4];
    unsigned int   result;
    int            i,j;
    unsigned char  octet;
```

Simulator Profiling

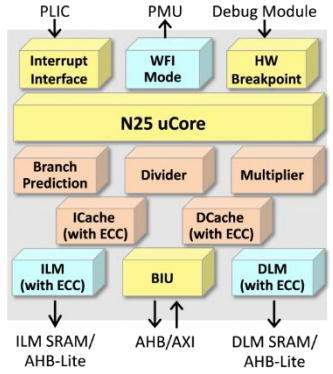
Total Self Cycle Count: 5574486

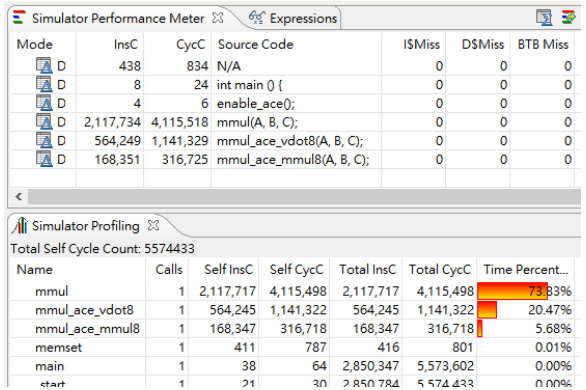
Name	Calls	Self InsC	Self CycC	Total InsC	Total CycC	Time Percent...
mmul	1	2,117,717	4,115,492	2,117,717	4,115,492	73.83%
mmul_ace_vdot8	1	564,245	1,141,310	564,245	1,141,310	20.47%
mmul_ace_mmul8	1	168,347	316,727	168,347	316,727	5.68%

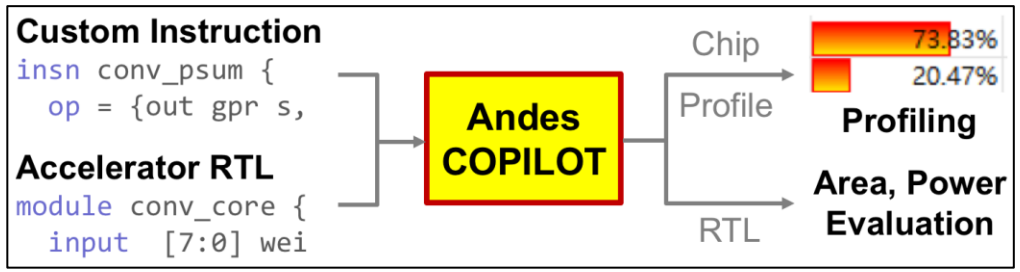


Research Outcomes

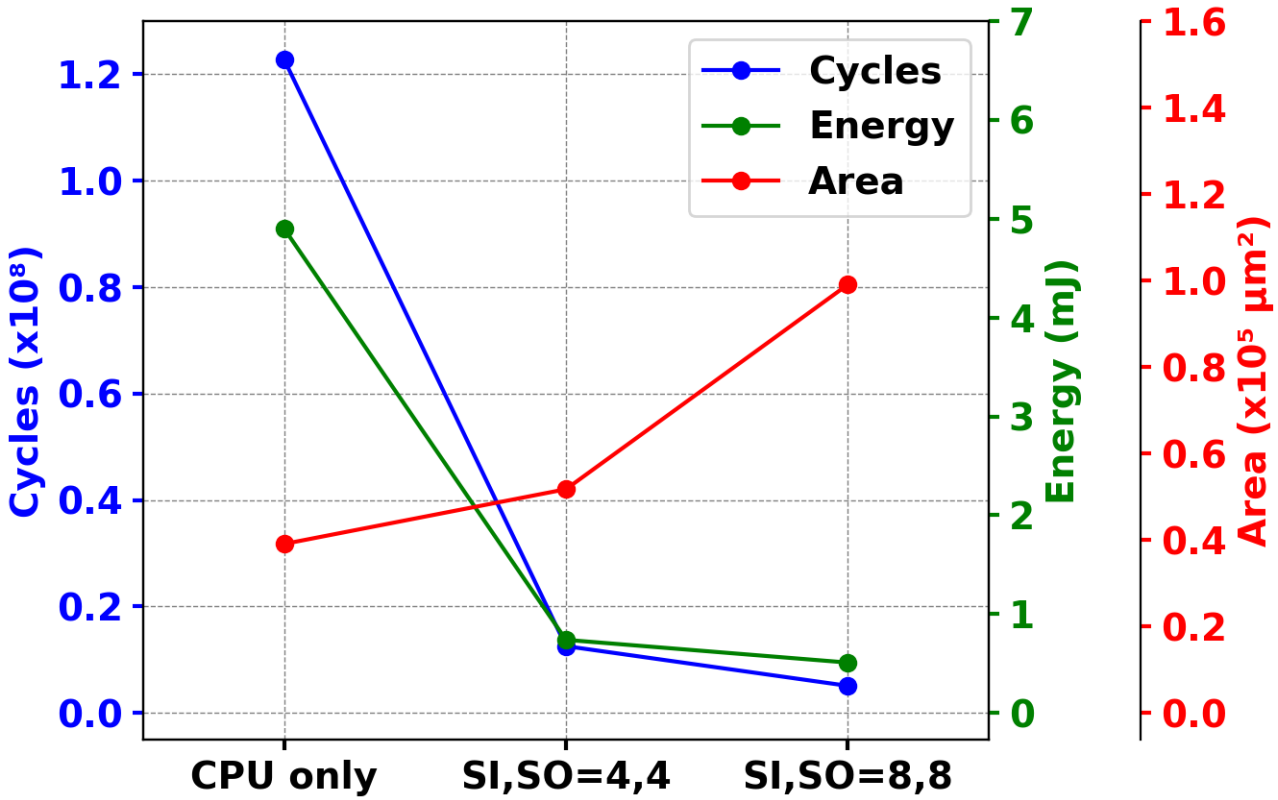
Platform: Andes N25, COPILOT







2D Convolution



* Evaluated in TSMC 40nm technology

- **(SI, SO):** input/output channel partition

  (4, 4): 9.8x speed up, 32% more area; **(8, 8)**: 24.1x speed up, 153% more area

We thank **Andes Technology** and **TSRI** for technical support