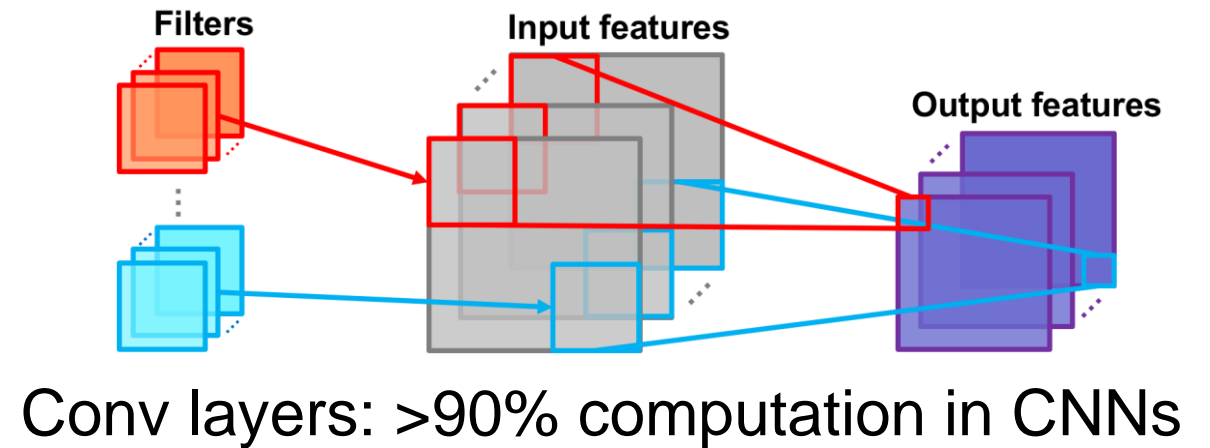
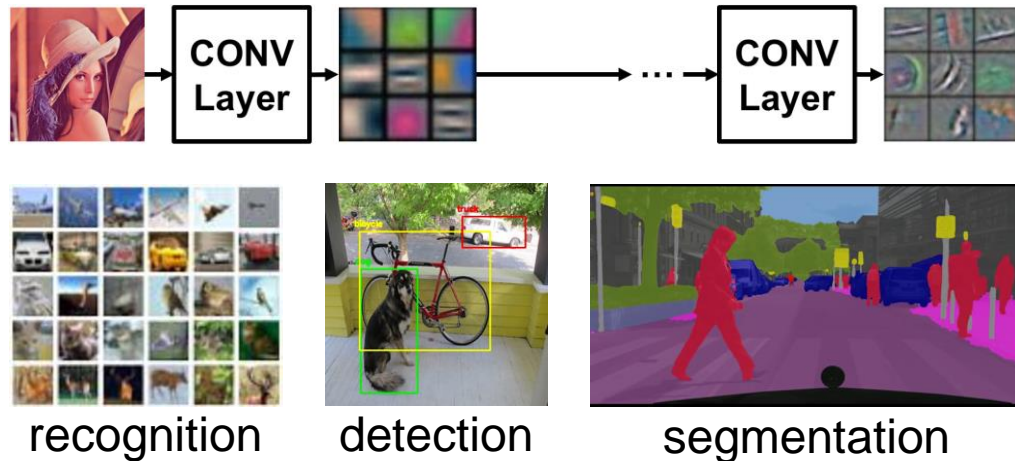


# Overview

- Applying RISC-V core with custom instructions to mobile AI



- Profiling RISC-V program with additional custom instructions
- Evaluating hardware performance for multiple configurations

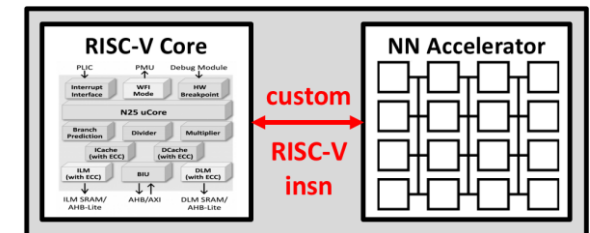
```

insn crc32 {
  op = {out gpr crc, in gpr data};
  csim = %{
    char      dat8b[4];
    unsigned int result;
    int       i, j;
    unsigned char octet;
  }
}
    
```

Simulator Profiling

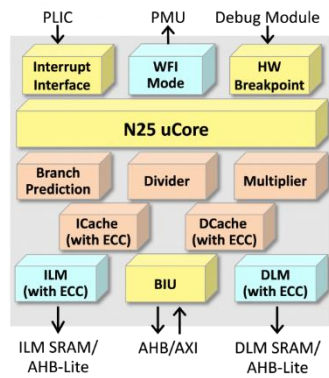
Total Self Cycle Count: 5574486

Name	Calls	Self InsC	Self CycC	Total InsC	Total CycC	Time Percent...
mmul	1	2,117,717	4,115,492	2,117,717	4,115,492	73.83%
mmul_ace_vdot8	1	564,245	1,141,310	564,245	1,141,310	20.47%
mmul_ace_mmul8	1	168,347	316,727	168,347	316,727	5.68%



# Research Outcomes

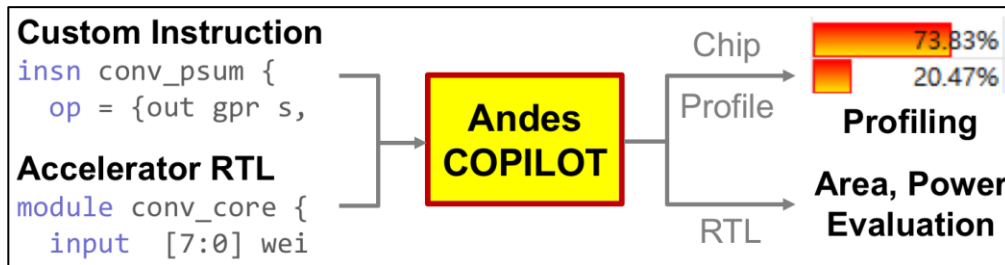
## Platform: Andes N25, COPILOT



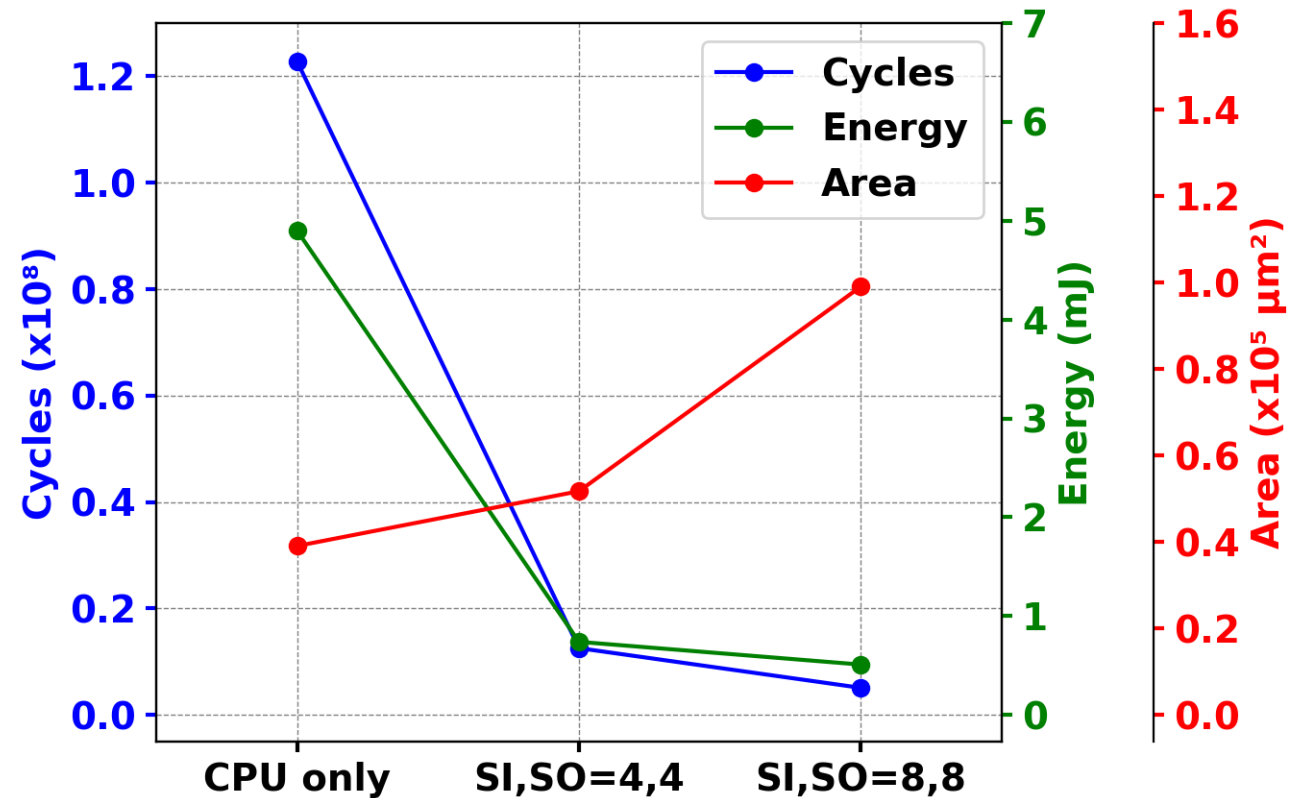
Mode	InsC	CycC	Source Code	ISMiss	DSMiss	BTB Miss
D	438	834	N/A	0	0	0
D	8	24	int main () {	0	0	0
D	4	6	enable_ace0;	0	0	0
D	2,117,734	4,115,518	mmul(A, B, C);	0	0	0
D	564,249	1,141,329	mmul_ace_vdot8(A, B, C);	0	0	0
D	168,351	316,725	mmul_ace_mmul8(A, B, C);	0	0	0

Name	Calls	Self InsC	Self CycC	Total InsC	Total CycC	Time Percent...
mmul	1	2,117,717	4,115,498	2,117,717	4,115,498	73.83%
mmul_ace_vdot8	1	564,245	1,141,322	564,245	1,141,322	20.47%
mmul_ace_mmul8	1	168,347	316,718	168,347	316,718	5.68%
memset	1	411	787	416	801	0.01%
main	1	38	64	2,850,347	5,573,602	0.00%
start	1	21	30	2,850,784	5,574,433	0.00%



## 2D Convolution



\* Evaluated in TSMC 40nm technology

- **(SI, SO):** input/output channel partition
- **(4, 4):** 9.8x speed up, 32% more area;    **(8, 8):** 24.1x speed up, 153% more area

We thank **Andes Technology** and **TSRI** for technical support

