#### **Innovation Unleashed: Solutions Enabling Embedded Intelligence**

SiFive China

**Si**Five

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### **Global Trends**



Source: Cisco VNI Global IP Traffic Forecast, 2017 - 2022



### SiFive Core IP Embedding Intelligence Everywhere



#### Consumer

AR/VR/Gaming devices Smart Home Imaging/Wearables

#### Storage/Networking/5G

SSD, SAN, NAS Base Stations, Small cells, APs Switches, Smart NICs, Offload cards



#### ML/Edge

Sensor Hubs, Gateways Autonomous machines IoT devices





### Embedding Intelligence from the Edge to the Cloud

#### SiFive Core IP 2 series:

SiFive's **smallest** and most **efficient** RISC-V processor IP



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### **Core IP 7 Series Standard Cores**

E76, E76-MC
S76, S76-MC
U74, U74-MC



Standard Cores represent pre-configured implementations of a Core Series which are available for free RTL and FPGA evaluations



#### SiFive 7 Series Embedded Intelligence Everywhere



In-cluster coherent combination of real-time and application processors



#### **Product Map**

	ECores 32-bit embedded cores MCU, edge computing, AI, IoT	<b>S Cores</b> 64-bit embedded cores Storage, AR/VR, machine learning	UCORES 64-bit application cores Linux, datacenter, network baseband
7 Series	E7 Series	S7 Series	U7 Series
Highest performance: 8-stage, dual-issue superscalar pipeline	> E76-MC Compare to Cortex-N Quad-core 32-bit embedded processor	<ul> <li>M7 &gt; S76-MC No 64-bit Cortex equivalent</li> <li>Quad-core 64-bit embedded processor</li> </ul>	<b>&gt; U74-MC</b> Compare to Cortex-A55 MP4 Multicore: four U74 cores and one S76 core
	E76 Compare to Cortex-M High performance 32-bit embedded core	A7 <b>&gt; S76</b> No 64-bit Cortex equivalent High-performance 64-bit embedded core	<b>&gt; U74</b> Compare to Cortex-A55 High performance Linux-capable processor
3/5 Series	E3 Series	S5 Series	U5 Series
Efficient performance: 5–6-stage, single- issue pipeline	<b>E34</b> Compare to Cortex-R: E31 features + single-precision floating points	5F       > S54       No 64-bit Cortex equivalent         Int       S51 features + single-precision floating point	> U54-MC Compare to Cortex-A53 Multicore application processor with four U54 cores and one S76 core
	E31 Compare to Cortex-R Balanced performance and efficiency	<ul> <li>R5 &gt; S51 No 64-bit Cortex equivalent Low-power 64-bit MCU core</li> </ul>	<b>&gt; U54</b> Compare to Cortex-A53 Linux-capable application processor
2 Series	E2 Series	S2 Series	
<b>Power &amp; area</b> optimized: 2–3-stage, single- issue pipeline	<b>E24</b> Compare to Cortex-M4 E21 + single-precision floating point	4F <b>S21</b> No 64-bit Cortex equivalent Area-efficient 64-bit MCU core	
	<ul> <li>E21 Compare to Cortex-M</li> <li>E20 + User Mode, Atomics, Multiply, TIM</li> </ul>	Λ4	
	> E20 Compare to Cortex-Mo Our smallest, most efficient core	0+	

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### Storage

**Coherent in-cluster combination** of application processors and real-time processors

**Configurable memory maps and coherent accelerator ports** for tightly coupling storage specific accelerators

**Optional FPU** for applications which don't need floating point capability Deterministic mode for FAST DATA applications with hard real-time constraints

Tightly integrated memories and Cache lock capability for critical real time workloads

Storage, ML, Cryptography specific **custom instructions** 

**64-bit real-time addressability** for **BIG DATA** applications



# **5G/Networking**

**Complex arithmetic** capability for accelerating baseband functions

**High bandwidth accelerator ports** for enabling intelligent offload processing

**Configurable memory maps** for optimizing QoS

In-cluster coherence of application and real-time processor enables 5G latency (<1ms) requirements

Hard real-time capabilities for scheduling baseband protocol layers

High throughput processing for next gen 5G stacks

Tightly Integrated Memories and Cache lock capability for critical real time workloads



## **AR/VR/Sensor Fusion**

Low Latency peripheral access and coherent accelerator port

**Combine** with SiFive 2, 3 or 5 series for designs with tight power constraints

**Coherent in-cluster combination** of application processors with real time processors

**Simple caching hierarchy** for ease of application optimization

Workload specific customizations (AR/VR/MR/CV)

Mixed precision arithmetic for accelerating machine learning compute



### **Enterprise SSD**

- FADU Annapurna SSD Controller
  - World's first RISC-V SSD controller
- FADU Bravo Series Enterprise SSD
- **3.5GB** throughput and **800K IOPS** at less than 1.8W
- Powered by SiFive E51

"SiFive's RISC-V Core IP was **1/3 the power** and **1/3 the area** of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products." J. Lee, FADU CEO



# **Intelligent Edge**

- Microsemi's PolarFire SoC
- World's first RISC-V SoC FPGA architecture bringing Real-time to Linux
- Targeted for **real-time Linux** applications at the Edge
- **Defense-grade** security features
  - Secure boot
  - DPA safe crypto core
  - SECDED on all memories
  - Physical memory protection/PMP
- Powered by SiFive U54-MC and SiFive E51



### Wearable AI

- Huangshan No. 1 (MHS001) from Huami using Upbeat Tech
- Integrated biometric signal processor with 4 dedicated AI engines and built-in CNN based inference engine
- **38 percent more efficient** than the Arm Cortex-M4
- Powered by SiFive E31

"The world's first artificial intelligence powered wearable chipset"





huami



#### SiFive Core IP: Embedded Intelligence Everywhere

#### Efficient Performance

#### Scalability

# Embedding intelligence for a world of a Trillion Connected Devices

#### Compelling Feature Set



### **Contact Us**

sales@sifive-china.com

marketing@sifive-china.com

recruitment@sifive-china.com



SiFive China Wechat



- Best in class in RISC-V based solution with local customer support
- Leader in RISC-V ecosystem development to support China semiconductor industry, growing with open-source community
- Pioneer in cloud-based SaaS service for custom ASICs.