RISC-V Technical Committee Update

ZÜRICH Workshop, June 2019

Silviu Chiricescu Draper Laboratory
Vice-Chair Technical Committee

Task Groups and Standing Committes	Chair	Vice-Chair	Status
Base ISA Ratification Task Group	Krste Asanovic	Andrew Waterman	RV32I, RV64I base , MFDQC std ext ratified (v2.x)
Privileged ISA Spec Task Group	Andrew Waterman	Krste Asanovic	M, S (v1.1) Specs ratified April 12, 2019
UNIX-Class Platform Spec Task Group	Palmer Dabbelt	Atish Patra	Started meetings April 2019
Formal Specification Task Group	Nikhil Rishiyur		Public review of the fomal spec contenders completed last month.
Compliance Task Group	Allen Baum	Stuart Hoad	Coverage metrics definition for RV32I & v1.3 of test spec
B Extension (Bit Manipulation) Task Group	Ken Dockser	Clifford Wolf	Version 0.9 published; binutils/simulators available
J Extension (Dynam. Translated Lang) TG	Martin Maas	David Chisnall	Proposals & draft spec to be presented at June workshop
P Extension (Packed-SIMD Inst) Task Grp	Chuanhua Chang	Eric Flamand	Spec review for detailed instruction ops; binutlis/simulator available
V Extension (Vector Ops) Task Group	Krste Asanovic	Roger Espasa	Version 0.7 published; binutils/simulators avalable
Cryptographic Extension Task Group	Richard Newell	Daniel Zimmerman	AES, SHA-2 to be presented at June workshop
Debug Specification Task Group	Tim Newsome	Ernie Edgar	Version 0.13 ratified in 2018. V0.14 WIP backward compatible
Fast Interrupts Spec Task Group	Krste Asanovic	Kevin Chen	Core-local interrupt controller (CLIC) v0.8 draft specificaiton
Memory Model Spec Task Group	Dan Lustig	Arvind	Spec ratified in 2018, TG wrapped, archived
Processor Trace Spec Task Group	Gajinder Panesar	Hugh O'Keefe	Draft spec available as of April 2019
Sv128 Specification Task Group	Steve Wallach		Stalled due to IP-related business issues
Trusted Execution Env Spec Task Group	Joe Xie	Nick Kossifidis	HW: PMP mods review done SW: secure monitor, boot arch WIP
Security Standing Committee	Helena Handschuh	Joe Kiniry	Speaker Program featuring best security researchers
Opcode Space Mgmt Standing Committee	Krste Asanovic	Andrew Waterman	First meeting TBD
Software Standing Committee	Arun Thomas	Palmer Dabbelt	Several tools released in April 2019

Base ISA

- RVWMO 2.0 – RISC-V Weak Memory Ordering is the default memory consistency model for RISC-V (2018)
- Since the RISC-V Summit the following extensions have been ratified:
  - RV32I/RV64I v2.1
  - Zifencei v2.0 – moved FENCE.I out of mandatory base and into a separate extension
  - Zicsr v2.0
  - M (v2.0), F, D, Q, C (all v2.2)
- A (v2.0) and ztso are *frozen*, but not ratified yet!

Privilege ISA

- Machine and Supervisor (v1.11) specs have been ratified

Formal Specification

- Multiple formal specifications each with its own strengths and limitations – no obvious winner.

	Forvis	Grift	Sail	riscv-plv	Kami
Link to description	Forvis	Grift	Sail	Riscv-plv	Kami
Author/Group	Bluespec	Galois	SRI/Cambridge	MIT	SiFive
Licence	MIT	GPL3	BSD	MIT	Apache 2.0
Metalanguage	Haskell	Haskell	Sail	Haskell	Kami/Coq
Functional coverage - Base ISA and extensions	RV32/64IMAFDC	RV32/64GC	RV32/RV64IMAC	RV32/64IMAF	RV32/64GC
Functional coverage - Privilege levels	MUS,Sv32,39,48	M	MUS,Sv32,39,48	Sv39	no

- Public review ended last month, but little feedback has been received
- Group is introspecting and discussing options on how to move forward– ideas are welcome!

Bit Manipulation – B Extension

- New draft spec (v0.9) has just been published and will be discussed at the workshop
- For all the instructions. proposed in the draft
  - C-intrinsics, binutil, spike support (courtesy of Symbiotic EDA), and binary simulator (from Imperas)

Packed SIMD - P Extension

- Initial draft specification (v0.5) released in April
- RV32/RV64 toolchain and (functional and timing) binary simulator (courtesy of Andes Technology) released last month
- Porting voice codecs and deep learning applications to evaluate the usefulness of the proposed instrs.

Vector – V Extensions

- Specification draft v0.7.1 to be released at the workshop
- Matching binutils and spike support (courtesy of SiFive) and a binary simulator (from Imperas)

Compliance

- Draft specification (v0.13) of the test format has been released last month
- Proposed definition of the coverage metrics for RV32IMC unprivileged instructions only
  - No code to measure the coverage on the existing tests
- New prototype framework being developed (Shakti project)

Processor Trace

- v0.26 released a few days ago
- C-reference code for encoder and decoder being worked on
- Patches to spike to include the above

Debug

- v0.13.2 had been ratified in 2018

Op Code Management Standing Committee

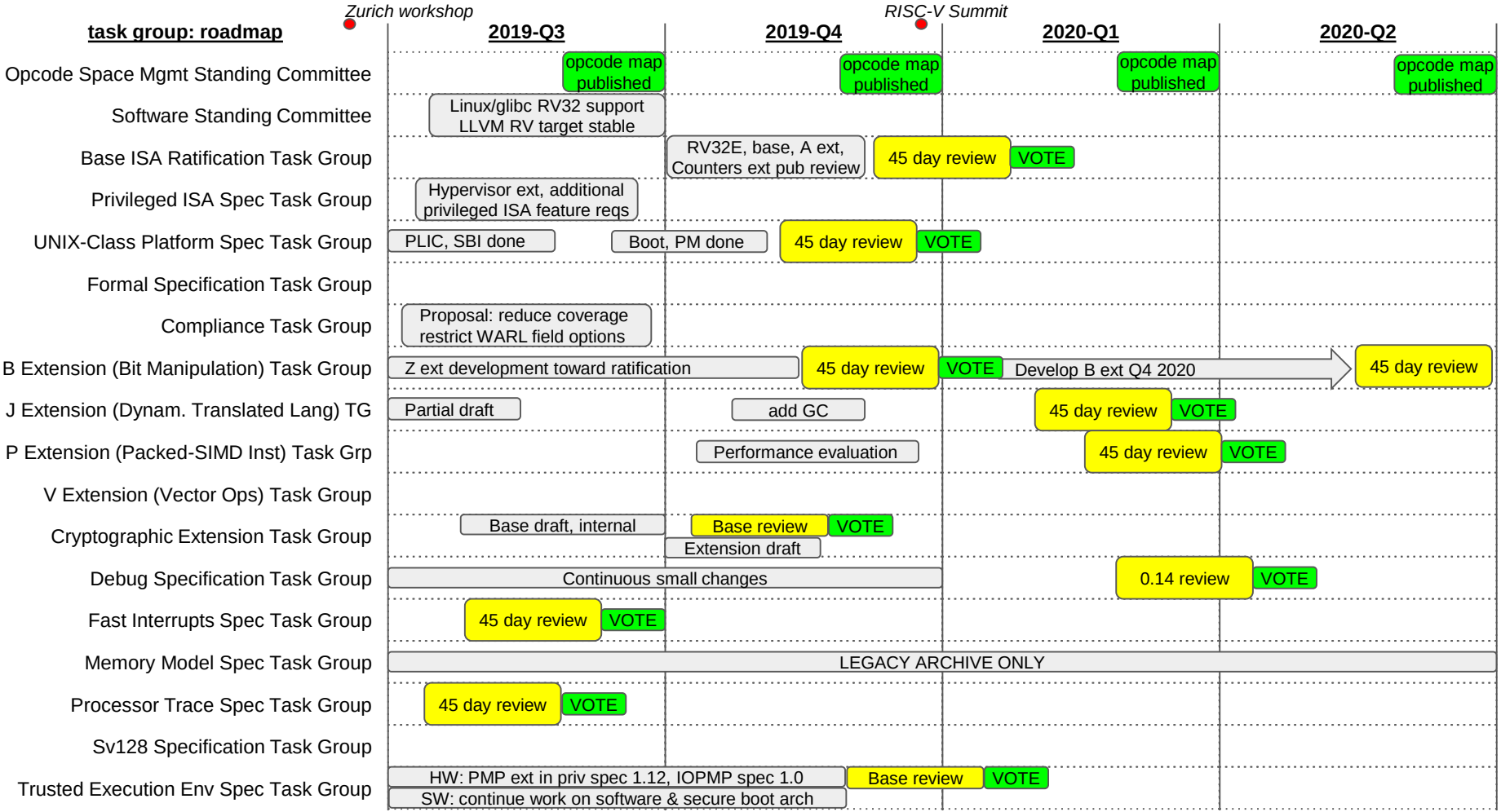
- Elevated from TG as there is a need to create a strategy/master plan for managing op cede requests from multiple TGs.

Security Standing Committee

- Identify and address challenges in security for the RISC-V based IoT devices, embedded systems, and machine learning implementations
- Develop consensus around best security practices for IoT devices and embedded systems
- Excellent Speaker Program
- Crypto Extensions TG
  - AES and SHA proposal to be presented at the workshop
- Trusted Execution Environment TG
  - PMP review, IOPMP extension
  - Secure monitor architecture definition, boot arch draft

Software Standing Committee

- Upstream OS support (i.e Fedora, Debian, FreeBSD, sel4, Zephyr, FreeRTOS)
- LLVM RV32/64 upstreamed and on track to become stable
- OpenSBI v0.3 released
- Rust v1.34 released last month (with RV32/64 support) – see the talk later on Wed.
- RISC-V sessions organized at different conferences (FOSDEM, Linux plumbers, etc.)
- Stable GNU Toolchain
  - Optimizing for code size and performance


Zurich workshop
RISC-V Summit
task group: roadmap
2019-Q3
2019-Q4
2020-Q1
2020-Q2
Opcode Space Mgmt Standing Committee
opcode map published
opcode map published
opcode map published
opcode map published
Software Standing Committee
Linux/glibc RV32 support
LLVM RV target stable
Base ISA Ratification Task Group
RV32E, base, A ext, Counters ext pub review
45 day review
VOTE
Privileged ISA Spec Task Group
Hypervisor ext, additional privileged ISA feature reqs
UNIX-Class Platform Spec Task Group
PLIC, SBI done
Boot, PM done
45 day review
VOTE
Formal Specification Task Group
Compliance Task Group
Proposal: reduce coverage restrict WARL field options
B Extension (Bit Manipulation) Task Group
Z ext development toward ratification
45 day review
VOTE
Develop B ext Q4 2020
45 day review
J Extension (Dynam. Translated Lang) TG
Partial draft
add GC
45 day review
VOTE
P Extension (Packed-SIMD Inst) Task Grp
Performance evaluation
45 day review
VOTE
V Extension (Vector Ops) Task Group
Cryptographic Extension Task Group
Base draft, internal
Base review
VOTE
Extension draft
Debug Specification Task Group
Continuous small changes
0.14 review
VOTE
Fast Interrupts Spec Task Group
45 day review
VOTE
Memory Model Spec Task Group
LEGACY ARCHIVE ONLY
Processor Trace Spec Task Group
45 day review
VOTE
Sv128 Specification Task Group
Trusted Execution Env Spec Task Group
HW: PMP ext in priv spec 1.12, IOPMP spec 1.0
Base review
VOTE
SW: continue work on software & secure boot arch

Call for participation/ownership

- *Provide feedback* on the draft specifications that are slated to be released for public review in the second half of 2019 - there are 6 of them!

- Software Stack development
  - Compiler code size
  - Support for the vector extensions
  - LLVM
  - Java
  - Browser (including Javascript VM)
  - Hypervisors