

# Building Secure Systems Using RISC-V and Rust



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RISC-V Workshop Zurich



RISC-V

# Talk Overview

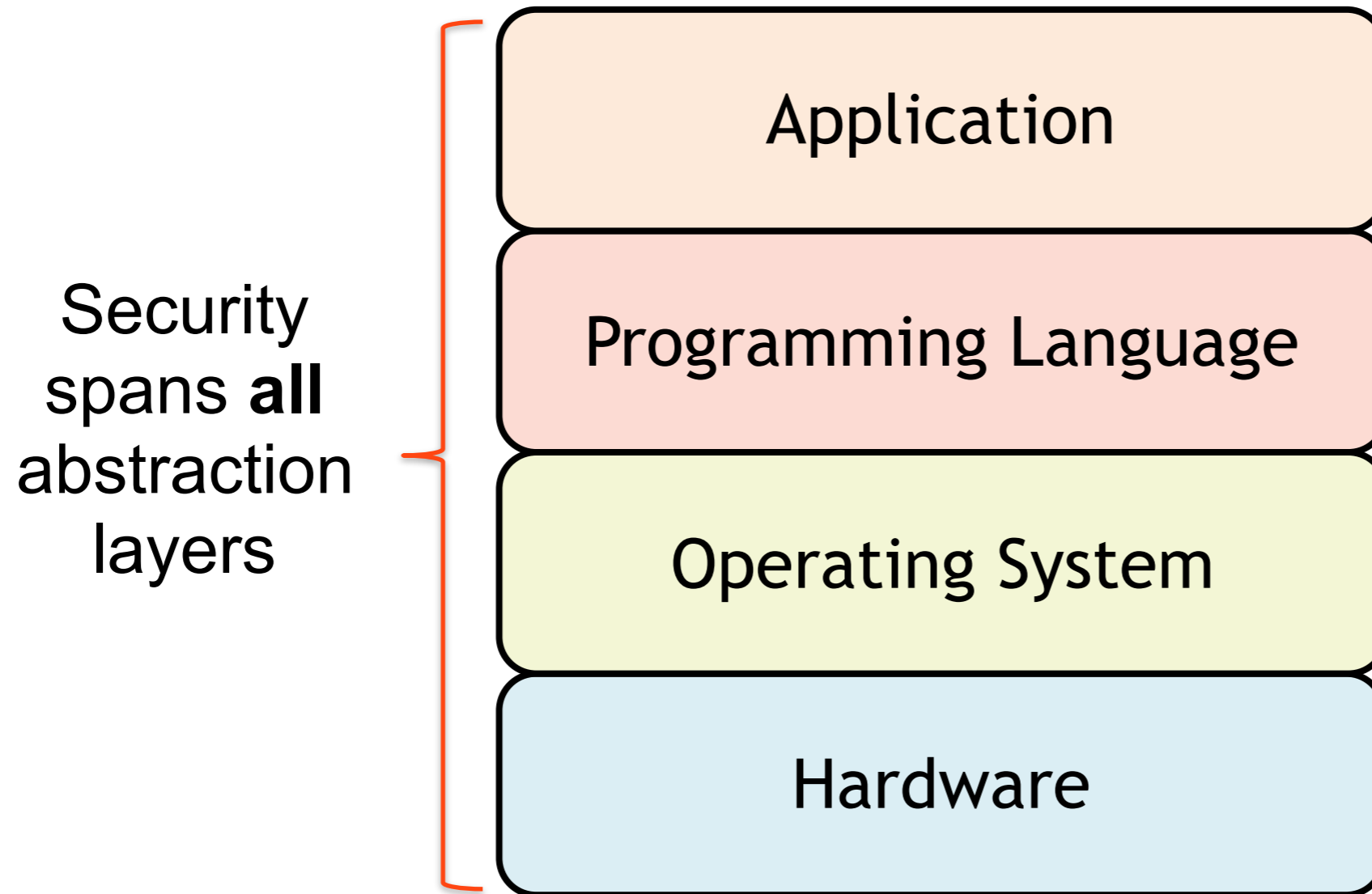
- How do you build a **secure computer system**?
- My take:
  - **RISC-V Hardware**: Openness, Simplicity, and Flexibility
  - **Rust Software**: Safety, Performance, and Productivity

How do you build a  
secure computer system?

Hint: Antivirus is **not** the answer.

(Ask Project Zero.)

# Securing Computer Systems



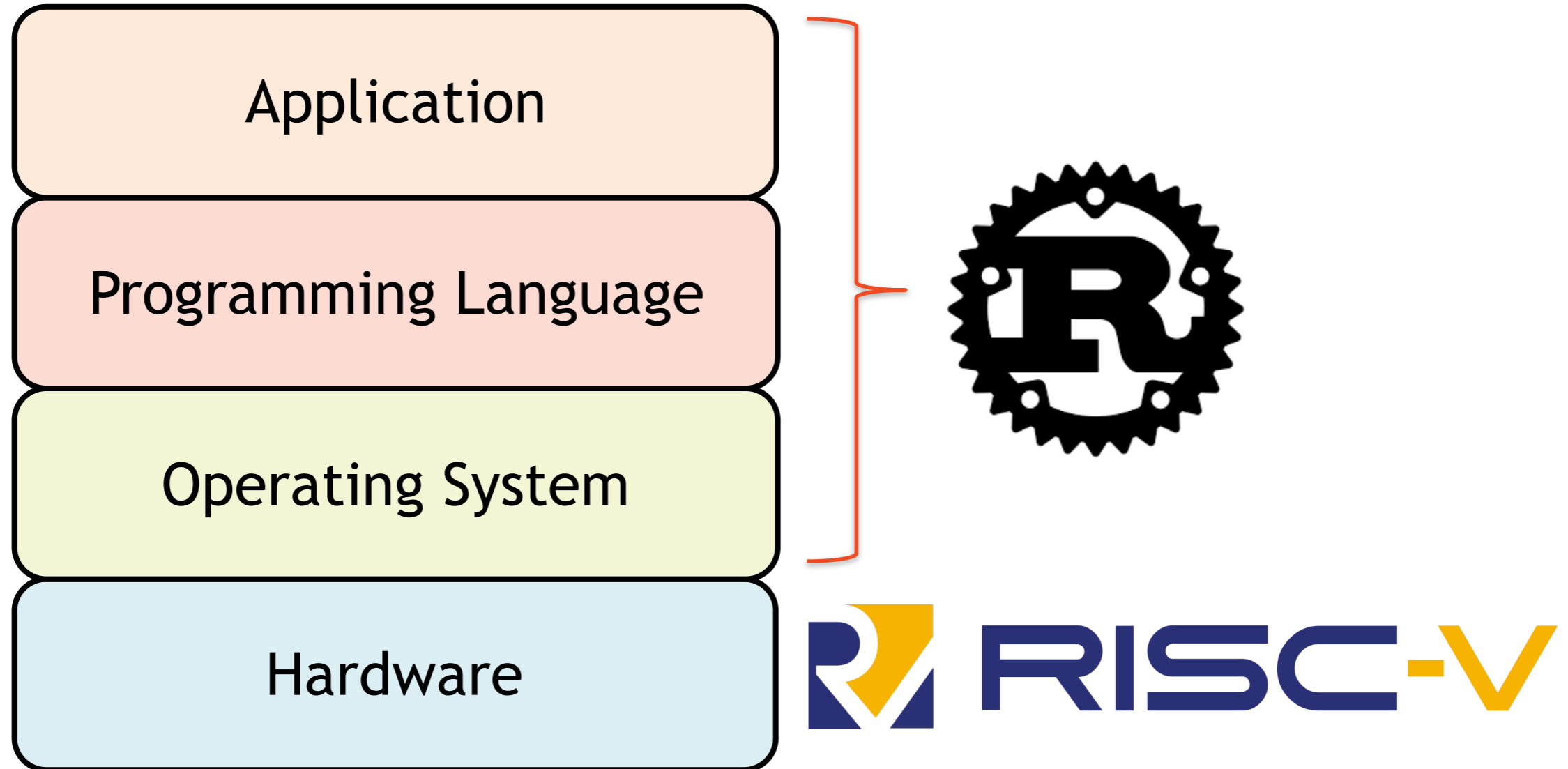
A flaw in **any layer** can compromise system security requirements.

# How Are We Doing?



Well, it turns out security is **HARD**.

# We Can Do Better



Building Secure Systems in the 21st Century:  
**RISC-V Hardware and Rust Software**



**RISC-V**



# RISC-V: **Opening Up** the Hardware Ecosystem

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- Several open RISC-V implementations exist
  - LowRISC, PULP, Chips Alliance, OpenHW, ...
- Industry and academia can collaborate more effectively
  - **No NDAs needed.** Just clone a git repo
  - Critical for making progress on solving hard security problems

*The RISC-V community has an **historic opportunity to “do security right”** from the get-go with the benefit of up-to-date knowledge.*

-RISC-V Foundation

# RISC-V as a **Platform** for Security Research

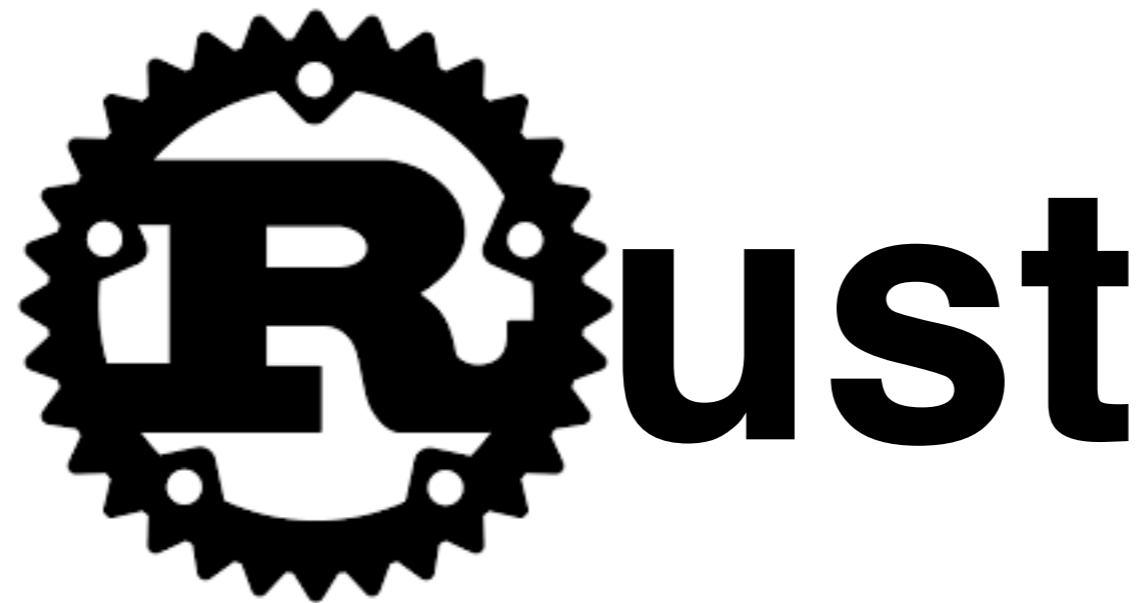
# RISC-V as a Platform for Security Research

- Several groups exploring new security ideas on RISC-V
  - Tagged Architectures (LowRISC, PIPE)
  - Hardware enforced capabilities (CHERI)
  - Formally verified RISC-V implementations (Kami)
  - Secure enclaves (Keystone, MI6)

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  - Secure enclaves (Keystone, MI6)
- More interesting work in the security session (post-break)





# On Systems Programming



*[A] systems programmer has seen the **terrors** of the world and understood the **intrinsic horror** of existence*

*-James Mickens, *The Night Watch**

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- Usually written in C or C++ for performance reasons
  - BUT C and C++ are **not memory-safe**
- **Memory corruption vulnerabilities** abound (and are exploited)
  - Microsoft study estimates 70% of security bugs are due to memory safety issues

It turns out programming languages have **evolved** in the last **50 years**.



Rust is a **safe,**  
**performant** systems  
programming language.



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- Mozilla began shipping Rust components in Firefox 48 in 2016
  - **Oxidization** is Mozilla's term for "Rusting out" components
- Rust code has improved Firefox's security and performance
  - **Security:** Safe parsers (e.g., New MP4 metadata parser replaced libstagefright)
  - **Performance:** New parallel CSS engine speeds up page loads

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- Excellent package manager and productive developer environment

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- Projects exploring Rust OS components for Linux kernel, FreeBSD kernel, seL4, and Fuchsia OS


# Rust/RISC-V



# Rust/RISC-V (RV32)

- RISC-V 32-bit support ([rust-embedded/wg#36](#), [rust-lang/rust#52787](#), [rust-lang/rust#53822](#)) released in Rust 1.30

**Closed** RISC-V Arch Support #36  
dvc94ch opened this Issue on Aug 21, 2017 · 39 comments

 japaric commented on Aug 3, 2018 Member ...

RISC-V support is now available in the latest nightly. You can compile crates for RISC-V using the `riscv32imac-unknown-none-elf` target and Cargo:

```
$ cargo new --lib foo
$ cd foo
$ cat src/lib.rs
```

```
#![no_std]

#![no_mangle]
pub fn foo(x: u32, y: u32) -> u32 {
    x + y
}
```

```
$ rustup target add riscv32imac-unknown-none-elf
$ cargo build --target riscv32imac-unknown-none-elf --release
$ cargo install cargo-binutils
$ cargo objdump -- -arch-name=riscv32 -d -no-show-raw-insn target/riscv32imac-unknown-none-elf/release/target/riscv32imac-unknown-none-elf/release/libfoo.rlib(foo-5f01dd28752961b9.foo0-d59093d565f158ef2f
```

Disassembly of section `.text.foo`:

```
foo:
    0:    add    a0, a1, a0
    4:    ret
```

# Rust/RISC-V (RV64)

- RISC-V 64-bit support ([rust-embedded/wg#218](#), [rust-lang/rust#58406](#) ) released in Rust 1.34

Add riscv64{imac,gc}-unknown-none-elf targets #58406 New issue

Merged bors merged 3 commits into `rust-lang:master` from `unknown repository` on Feb 15

Conversation 26 Commits 3 Checks 1 Files changed 6 +69 -1

 Disasm commented on Feb 12 Contributor

Previous attempt by @fintelia: #58012

Related: [rust-embedded/wg#218](#)

 4

 Disasm added some commits on Feb 12

-  Update LLVM: apply patches for RISC-V 64-bit support 0f4668a
-  Add riscv64imac-unknown-none-elf target 06f21a5
-  Add riscv64gc-unknown-none-elf target ✓ 1f1a824

 rust-highfive assigned **estebank** on Feb 12

Reviewers  
No reviews

Assignees  
 estebank

Labels  
S-waiting-on-bors  
T-compiler  
merged-by-bors  
relnotes

Projects  
None yet

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  - E.g., “hello world” to UART

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  - <https://github.com/riscv-rust/riscv-rust-quickstart>
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- See my Oxidize '19 talk for more details

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  - Important for Linux distributions and Firefox port
  - Help Wanted
- Tock microcontroller OS port in progress
  - Tock is written in Rust and provides a secure foundation for IoT devices

# Summary

- **RISC-V and Rust provide a strong foundation for building secure systems by combining:**
  - Safety, performance, and productivity of Rust
  - Openness, simplicity, and flexibility of RISC-V



**RISC-V**

