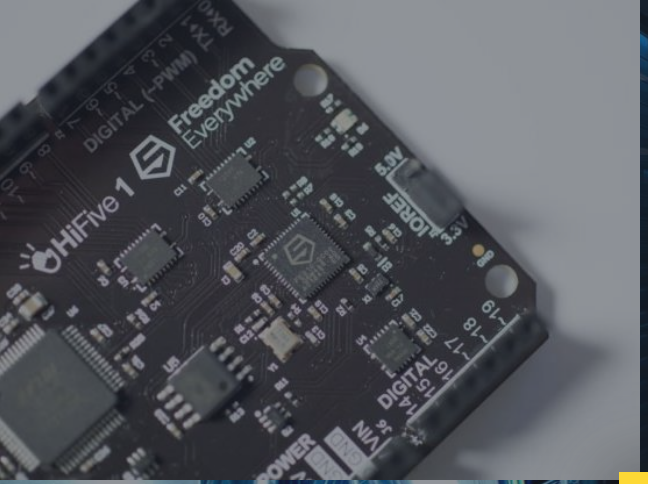


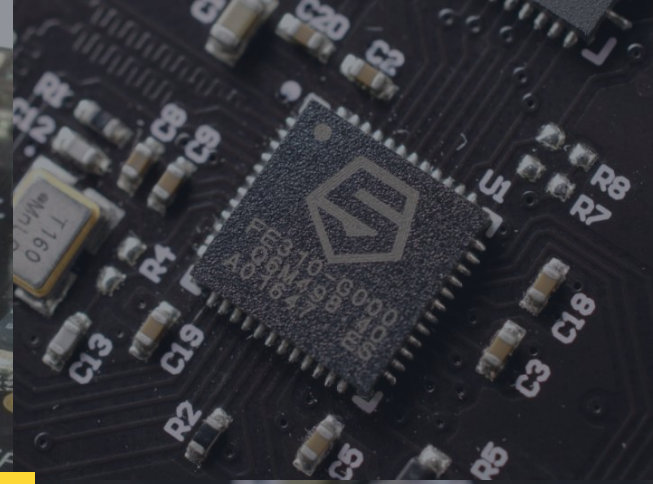


Embedded Intelligence Everywhere

James Prior

Product Marketing Communications

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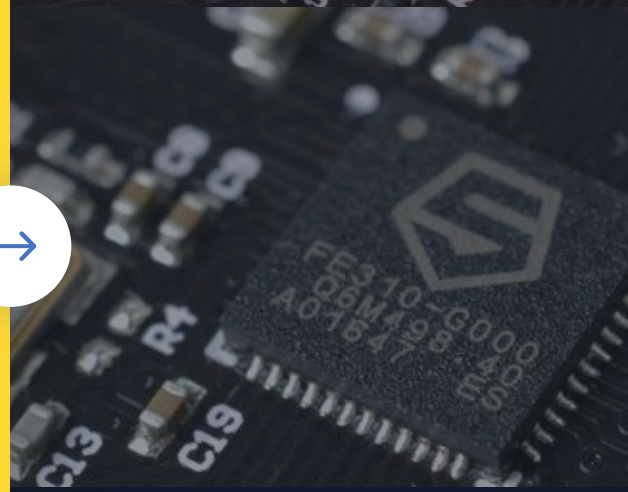
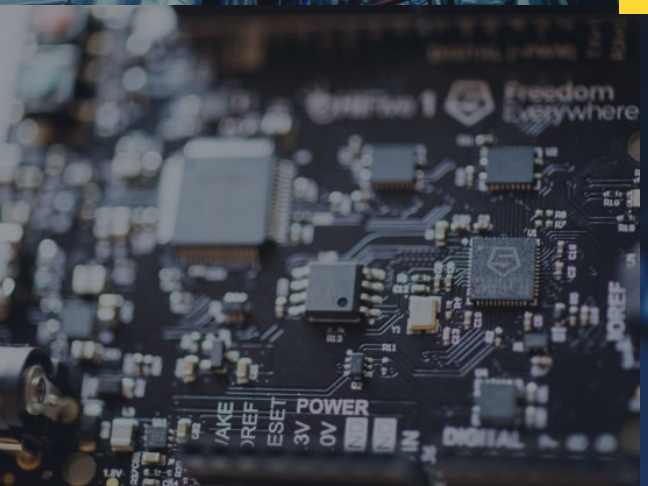
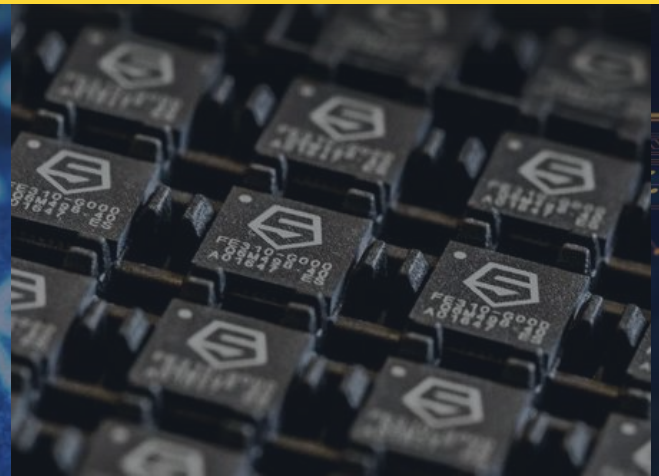
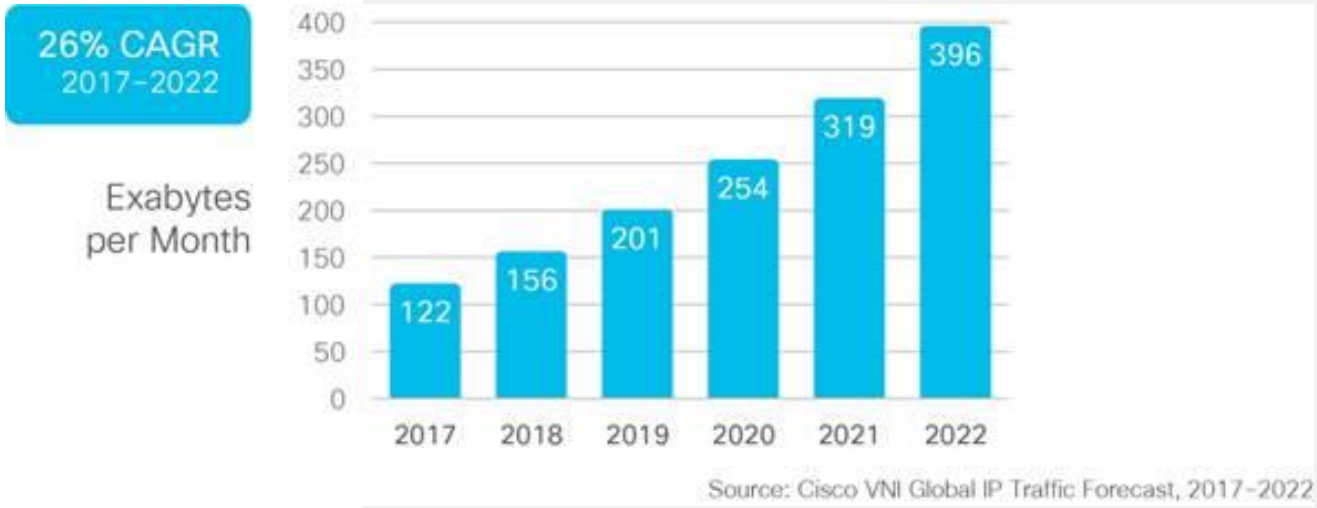
SiFive

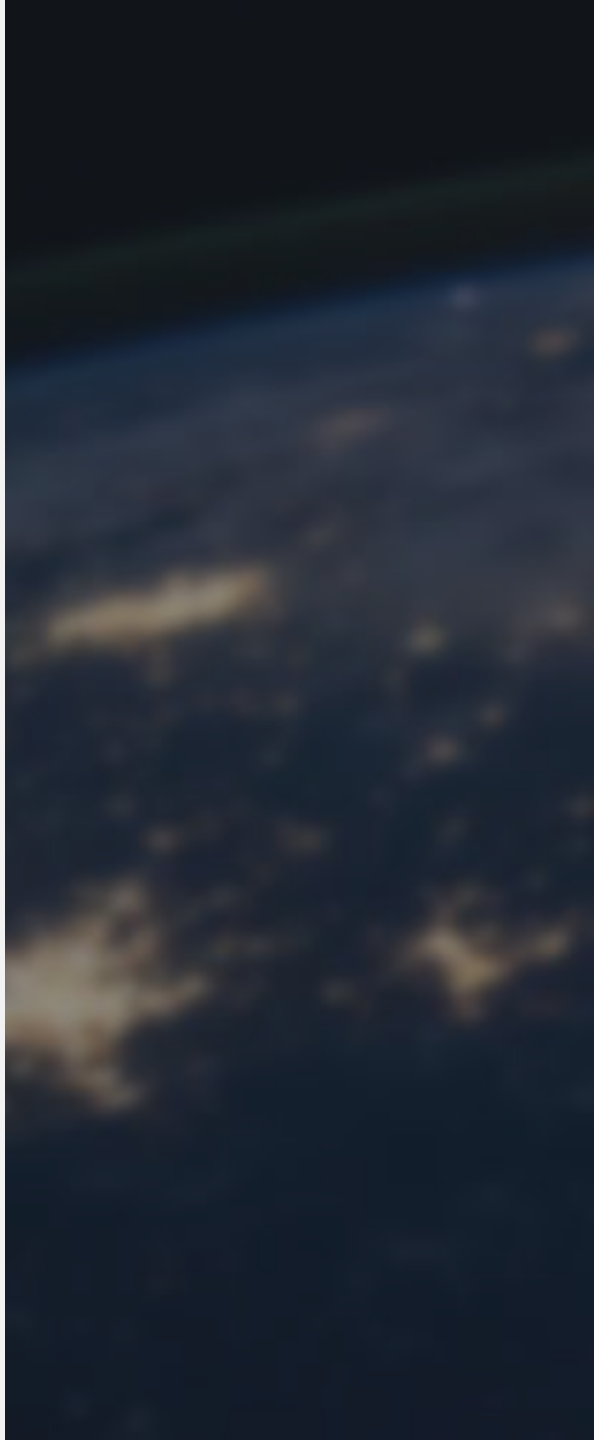



Global Trends

Internet users by 2022	Internet traffic by 2022	Devices/connections by 2022
60%	85 GB	3.6
of the population will be using the Internet *up from 45% in 2017*	of Internet traffic per month, per user *up from 29 GB in 2017*	networked devices and connections per person *up from 2.4 in 2017*



Source: Cisco VNI Global IP Traffic Forecast, 2017–2022



SiFive

SiFive Core IP
Embedding Intelligence Everywhere

Consumer

AR/VR/Gaming devices

Smart Home

Imaging/Wearables

Storage/Networking/5G

SSD, SAN, NAS

Base Stations, Small cells, APs

Switches, Smart NICs, Offload cards

ML/Edge

Sensor Hubs, Gateways

Autonomous machines

IoT devices

SiFive

SiFive 7 Series Core IP

The **highest performance** commercial **RISC-V** processor IP

SiFive

Core IP 7 Series
Standard Cores

01 **E76, E76-MC**

02 **S76, S76-MC**

03 **U74, U74-MC**

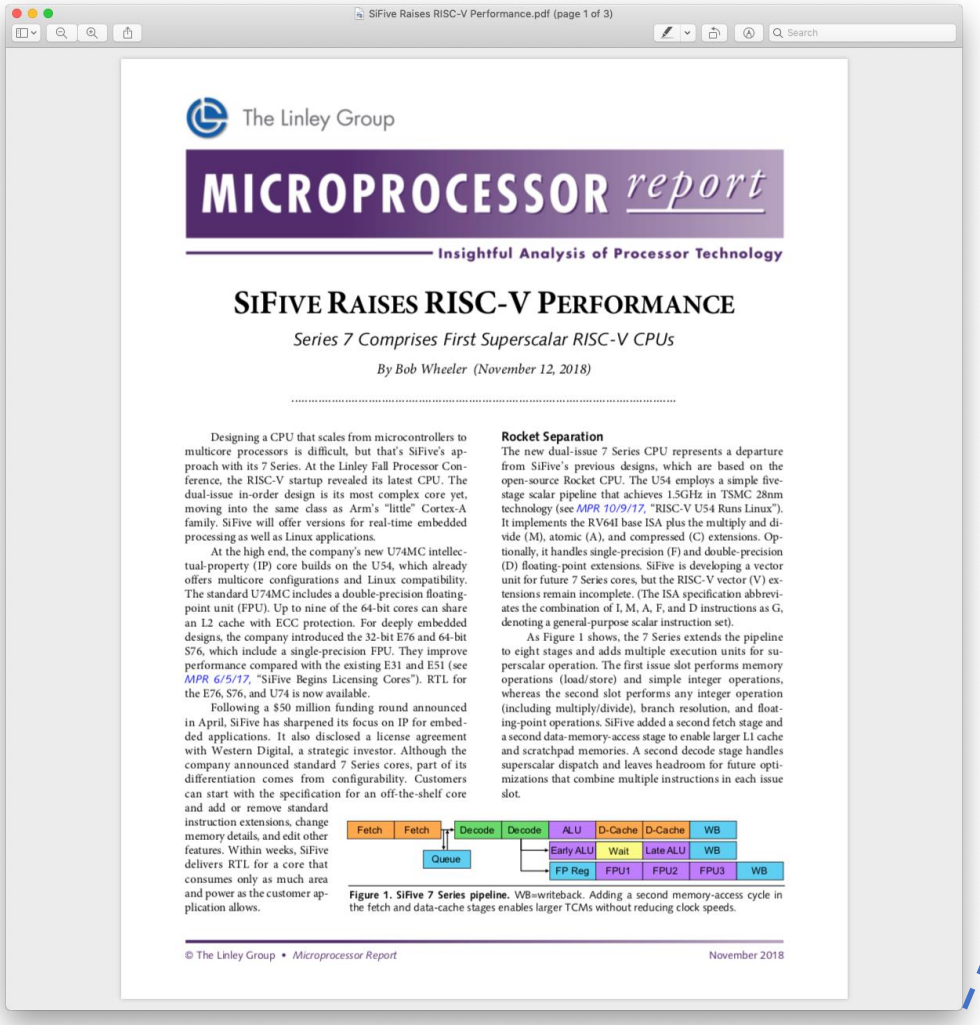
> Standard Cores represent **pre-configured implementations of a Core Series** which are available for free RTL and FPGA evaluations

SiFive

SiFive Core IP Portfolio

	E Cores — 32-bit embedded cores: MCU, edge computing, AI, IoT	S Cores — 64-bit embedded cores: Storage, AR/VR, machine learning	U Cores — 64-bit application cores: Linux, datacenter, network baseband
7 Series — **Highest performance:** 8-stage, dual-issue superscalar pipeline	**E7 Series**	**S7 Series**	**U7 Series**
	E76-MC — Compare to Cortex-M7 Quad-core 32-bit embedded processor	**S76-MC** — No 64-bit Cortex equivalent Quad-core 64-bit embedded processor	**U74-MC** — Compare to Cortex-A55 MP4 Multicore: four U74 cores and one S76 core
	E76 — Compare to Cortex-M7 High performance 32-bit embedded core	**S76** — No 64-bit Cortex equivalent High-performance 64-bit embedded core	**U74** — Compare to Cortex-A55 High performance LInux-capable processor
3/5 Series — **Efficient performance:** 5–6-stage, single-issue pipeline	**E3 Series**	**S5 Series**	**U5 Series**
	E34 — Compare to Cortex-R5F E31 features + single-precision floating point	**S54** — No 64-bit Cortex equivalent S51 features + single-precision floating point	**U54-MC** — Compare to Cortex-A53 Multicore application processor with four U54 cores and one S76 core
	E31 — Compare to Cortex-R5 Balanced performance and efficiency	**S51** — No 64-bit Cortex equivalent Low-power 64-bit MCU core	**U54** — Compare to Cortex-A53 Linux-capable application processor
2 Series — **Power & area optimized:** 2–3-stage, single-issue pipeline	**E2 Series**	**S2 Series**	
	E24 — Compare to Cortex-M4F E21 + single-precision floating point	**S21** — No 64-bit Cortex Equivalent Area optimized 64-bit processor	
	E21 — Compare to Cortex-M4 E20 + User Mode, Atomics, Multiply, TIM		
	E20 — Compare to Cortex-M0+ Our smallest, most efficient core		

7-Series Core IP – Efficient Performance vs. Legacy ISA



SiFive Raises RISC-V Performance.pdf (page 1 of 3)

The Linley Group

MICROPROCESSOR report

Insightful Analysis of Processor Technology

SiFive Raises RISC-V Performance

Series 7 Comprises First Superscalar RISC-V CPUs

By Bob Wheeler (November 12, 2018)

Designing a CPU that scales from microcontrollers to multicore processors is difficult, but that's SiFive's approach with its 7 Series. At the Linley Fall Processor Conference, the RISC-V startup revealed its latest CPU. The dual-issue in-order design is its most complex core yet, moving into the same class as Arm's "little" Cortex-A family. SiFive will offer versions for real-time embedded processing as well as Linux applications.

At the high end, the company's new U74MC intellectual-property (IP) core builds on the U54, which already offers multicore configurations and Linux compatibility. The standard U74MC includes a double-precision floating-point unit (FPU). Up to nine of the 64-bit cores can share an L2 cache with ECC protection. For deeply embedded designs, the company introduced the 32-bit E76 and 64-bit S76, which include a single-precision FPU. They improve performance compared with the existing E31 and E51 (see *MPR 6/5/17*, "SiFive Begins Licensing Cores"). RTL for the E76, S76, and U74 is now available.

Following a $50 million funding round announced in April, SiFive has sharpened its focus on IP for embedded applications. It also disclosed a license agreement with Western Digital, a strategic investor. Although the company announced standard 7 Series cores, part of its differentiation comes from configurability. Customers can start with the specification for an off-the-shelf core and add or remove standard instruction extensions, change memory details, and edit other features. Within weeks, SiFive delivers RTL for a core that consumes only as much area and power as the customer application allows.

Rocket Separation

The new dual-issue 7 Series CPU represents a departure from SiFive's previous designs, which are based on the open-source Rocket CPU. The U54 employs a simple five-stage scalar pipeline that achieves 1.5GHz in TSMC 28nm technology (see *MPR 10/9/17*, "RISC-V U54 Runs Linux"). It implements the RV64I base ISA plus the multiply and divide (M), atomic (A), and compressed (C) extensions. Optionally, it handles single-precision (F) and double-precision (D) floating-point extensions. SiFive is developing a vector unit for future 7 Series cores, but the RISC-V vector (V) extensions remain incomplete. (The ISA specification abbreviates the combination of I, M, A, F, and D instructions as G, denoting a general-purpose scalar instruction set).

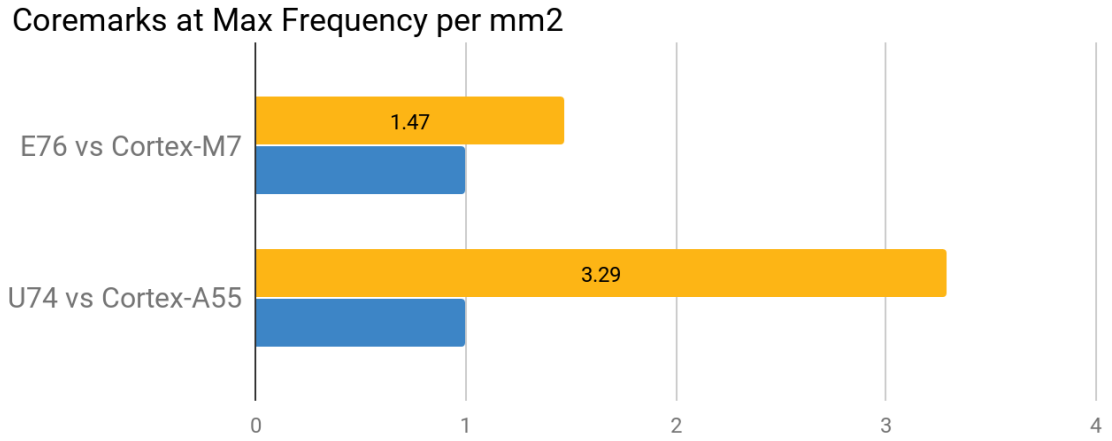
As Figure 1 shows, the 7 Series extends the pipeline to eight stages and adds multiple execution units for superscalar operation. The first issue slot performs memory operations (load/store) and simple integer operations, whereas the second slot performs any integer operation (including multiply/divide), branch resolution, and floating-point operations. SiFive added a second fetch stage and a second data-memory-access stage to enable larger L1 cache and scratchpad memories. A second decode stage handles superscalar dispatch and leaves headroom for future optimizations that combine multiple instructions in each issue slot.

Figure 1. SiFive 7 Series pipeline. WB=writeback. Adding a second memory-access cycle in the fetch and data-cache stages enables larger TCMs without reducing clock speeds.

 November 2018

	SiFive E76	Arm Cortex-M7	SiFive U74	Arm Cortex-A55
Instruction Set	32-bit RISC-V	32-bit Arm v7-M	64-bit RISC-V	64-bit Arm v8
Max Clock Freq	1.6GHz†	1.1GHz	1.6GHz†	1.6GHz†
Max IPC	2 IPC	2 IPC	2 IPC	2 IPC
CoreMark Perf	4.9CM/MHz	5.0CM/MHz	4.9CM/MHz	4.4CM/MHz†
Die Area*	0.065mm²	0.067mm²	0.22mm²	0.65mm²†

Table 1. SiFive-versus-Arm CPU comparison. The new dual-issue 7 Series delivers integer performance on a par with that of Arm's comparable CPUs. All metrics assume TSMC 28nm HP technology. *Without memories. (Source: vendors, except †The Linley Group estimate)



source : https://www.linleygroup.com/mpr/

SiFive Mix + Match Architecture?

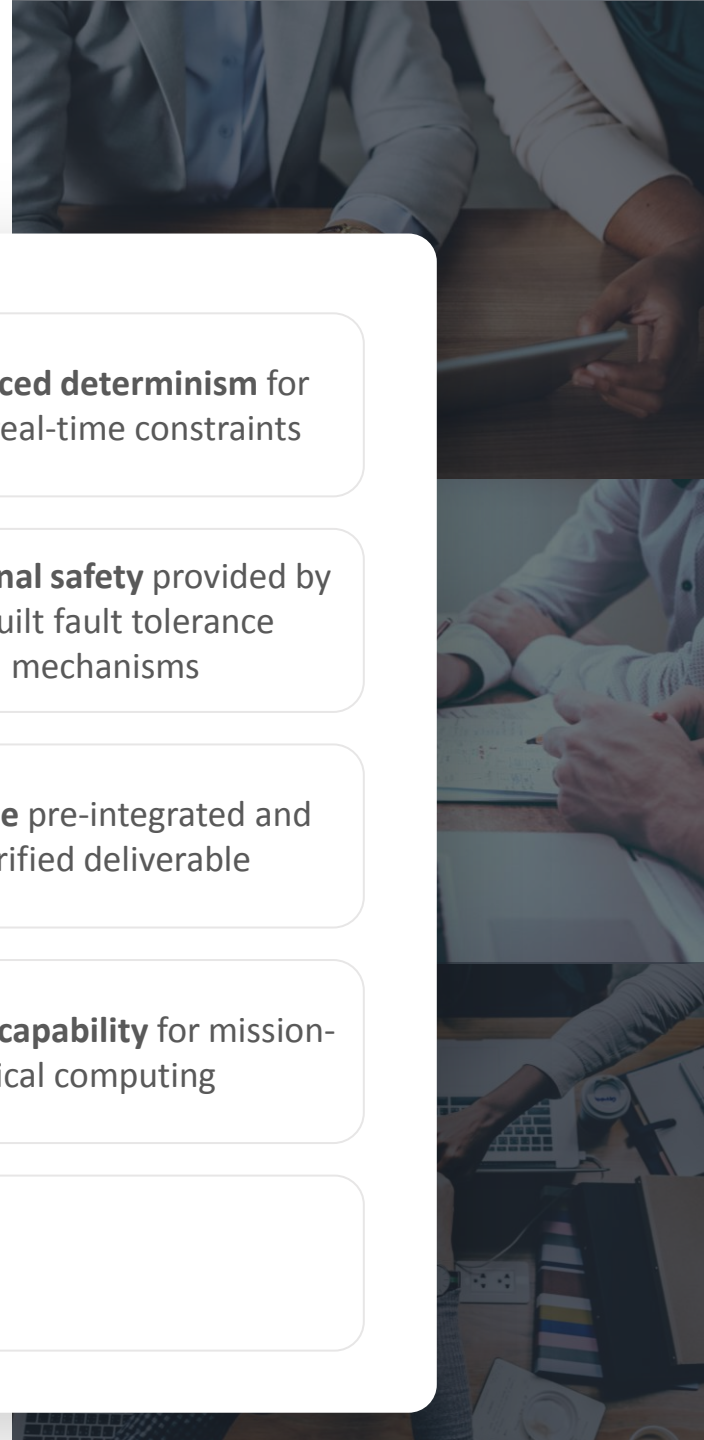
Efficiency

- Configure and use the right core for the job
- Power down large cores and memories when not needed

Performance

- Instant response times with real-time capable cores
- High-performance compute available when needed

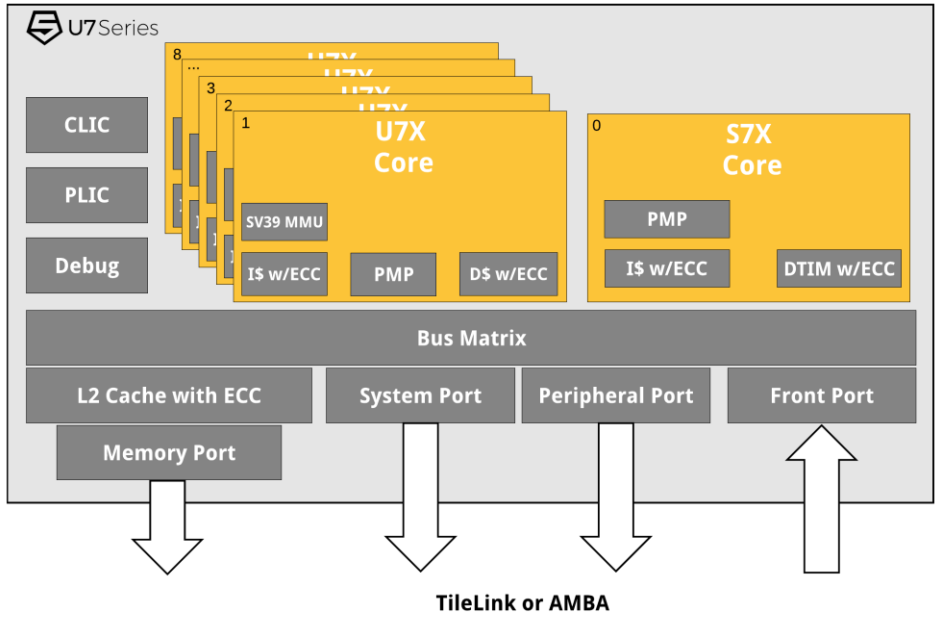
SiFive 7 Series
Embedded Intelligence Everywhere



Scalable throughput provided by **8+1** cores per cluster

Extensible design via custom instructions

Configurable memory architecture for application specific tuning



Enhanced determinism for hard real-time constraints

Functional safety provided by in-built fault tolerance mechanisms

A **single** pre-integrated and verified deliverable

Tightly integrated memory for low latency access

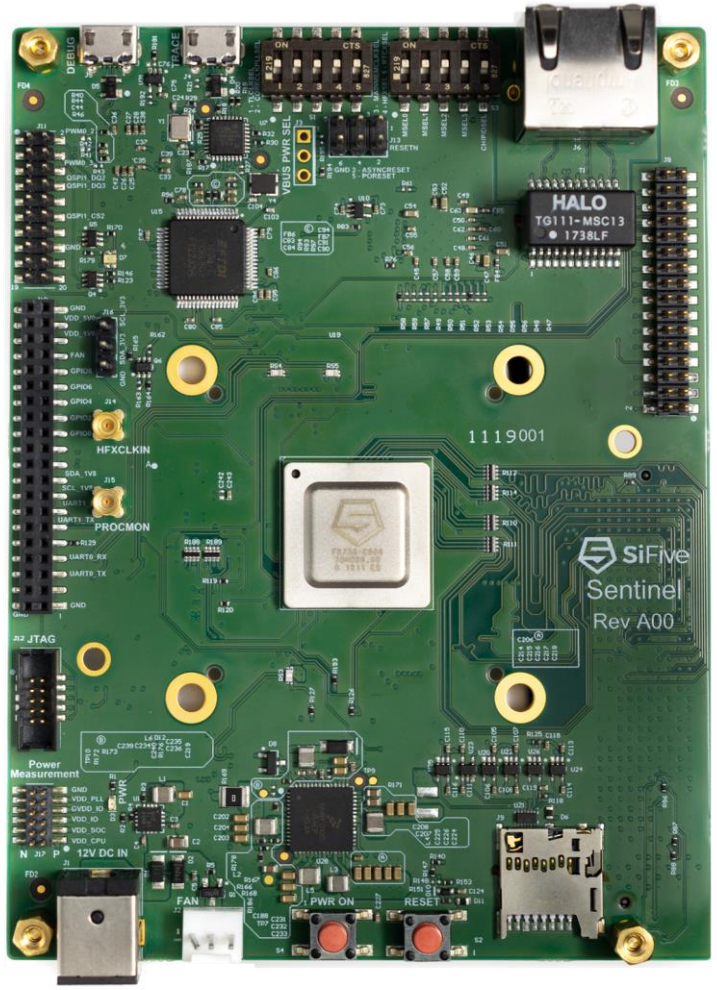
64-bit addressability for real time latency sensitive applications

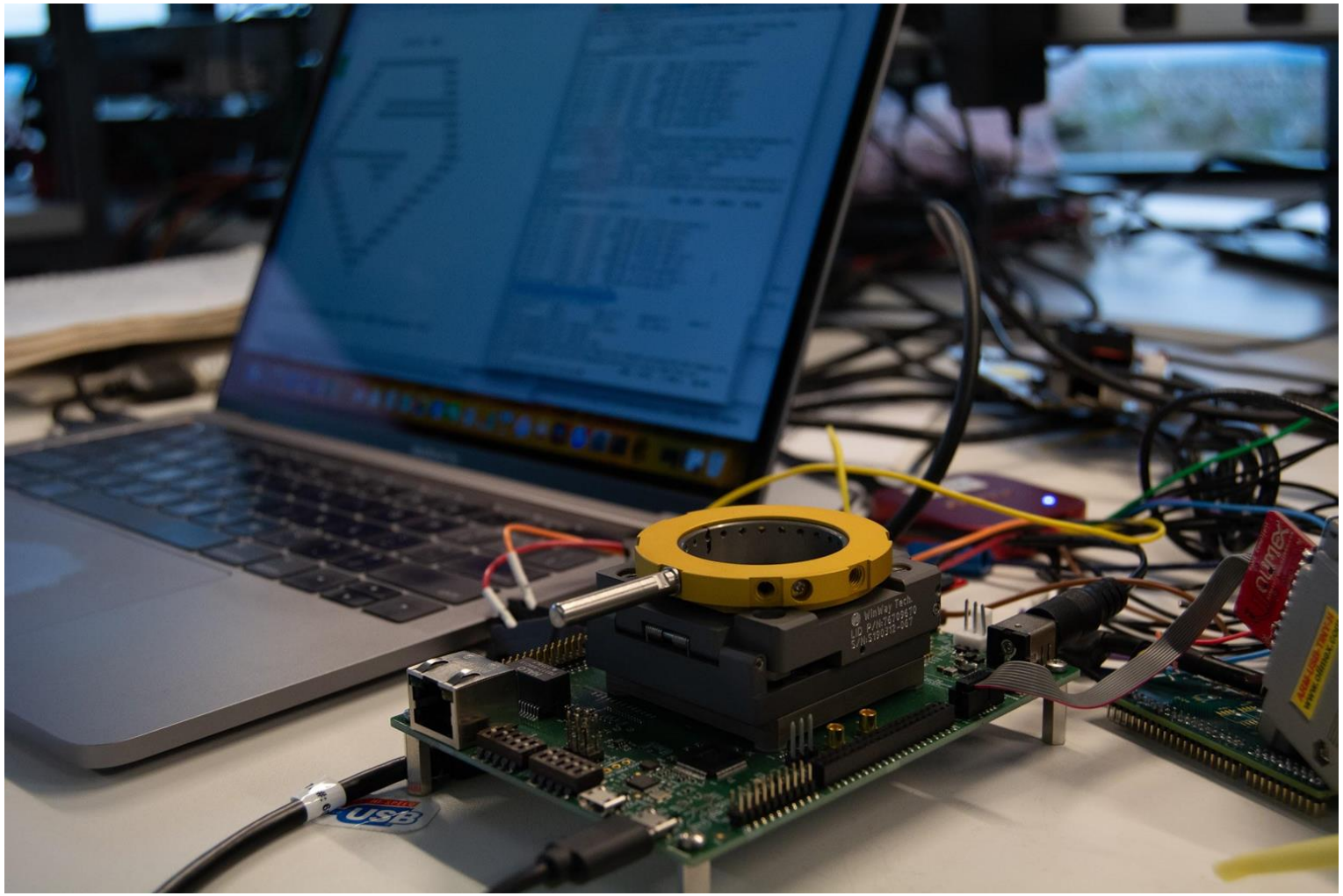
Mixed-precision arithmetic for efficient compute of ML workloads

Cache lock capability for mission-critical computing

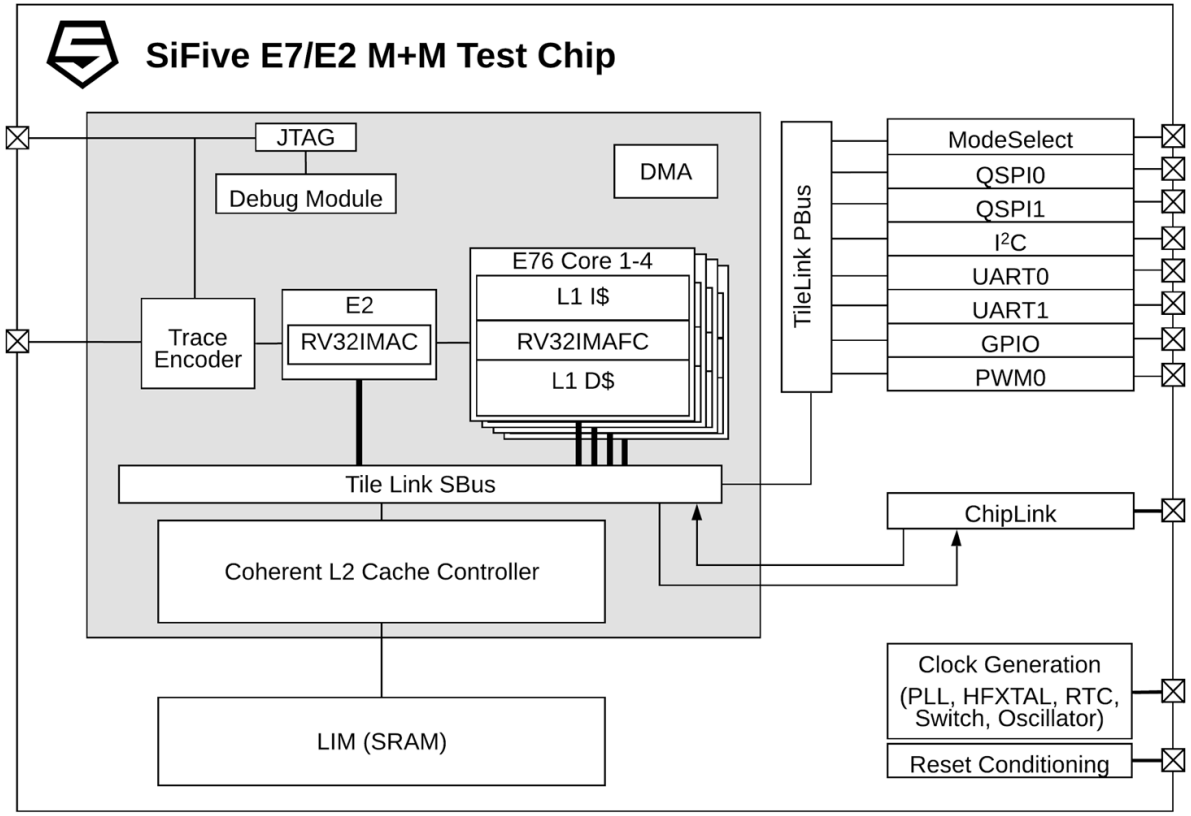
In-cluster coherent combination of real-time and application processors

7-Series Core IP Proven in Silicon





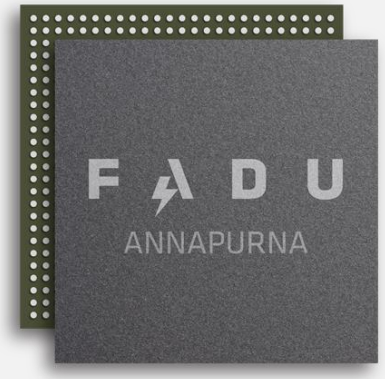
Showcasing SiFive Mix+Match Architecture



- **Heterogeneous Multicore**
  - 4x SiFive E76 Cores
  - 1x SiFive E21 Core
- **Coherent L2 Memory Subsystem**
  - L2 Cache with way-locking and directly addressable memory
  - Large cacheable SRAM on chip
- **Instruction Trace**
  - SiFive RISC-V silicon with instruction trace capabilities
- **ChipLink**
  - Coherent off-chip access

Enterprise SSD

- FADU Annapurna SSD Controller
  - **World's first** RISC-V SSD controller
- FADU Bravo Series Enterprise SSD
- **3.5GB** throughput and **800K IOPS** at less than 1.8W
- Powered by **SiFive E51**

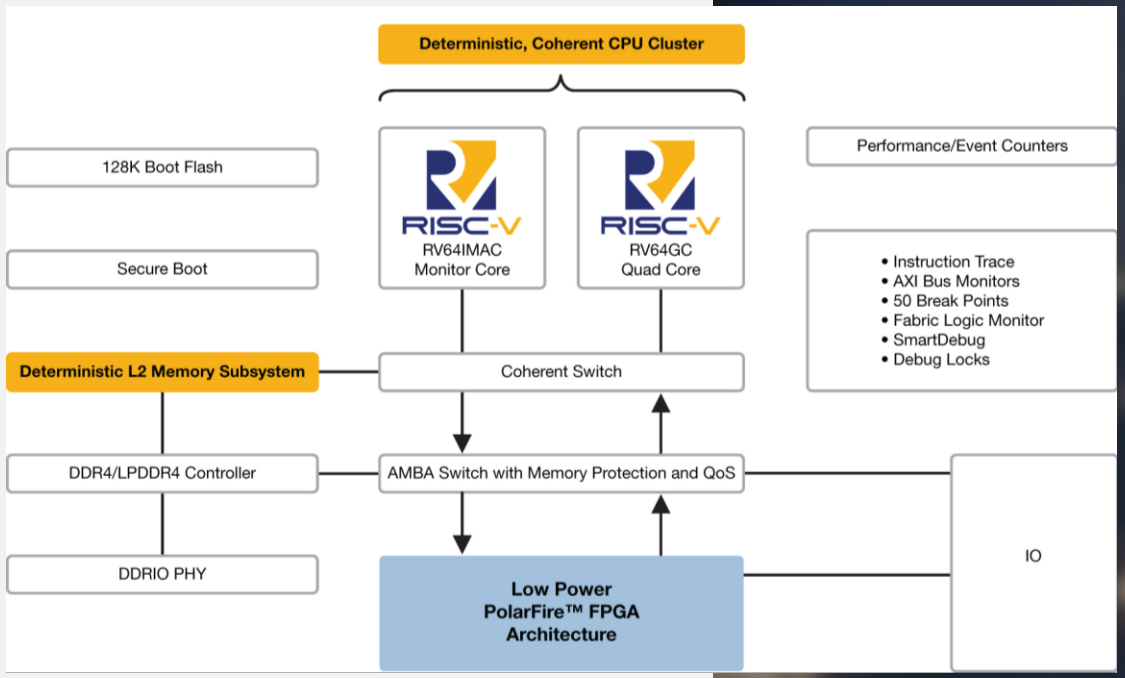


"SiFive's RISC-V Core IP was **1/3 the power** and **1/3 the area** of competing solutions, and gave FADU the flexibility we needed in optimizing our architecture to achieve these groundbreaking products." J. Lee, FADU CEO

FADU

Intelligent Edge

- Microsemi's **PolarFire SoC**
- **World's first RISC-V SoC FPGA architecture** bringing Real-time to Linux
- Targeted for **real-time Linux** applications at the Edge
- **Defense-grade** security features
  - Secure boot
  - DPA safe crypto core
  - SECDED on all memories
  - Physical memory protection/PMP
- Powered by **SiFive U54-MC and SiFive E51**

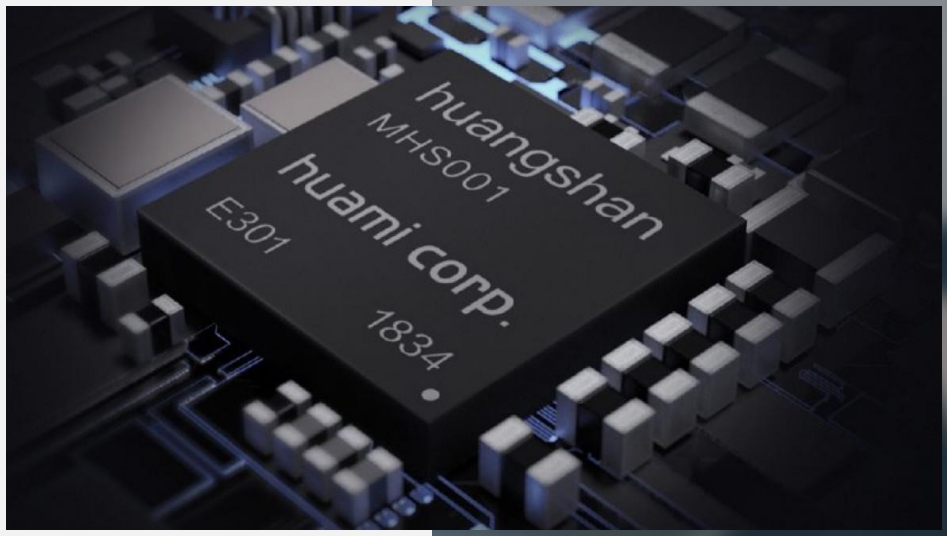


Microsemi
a Microchip company

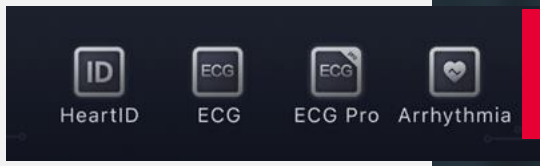
SiFive

Wearable AI

- **Huangshan No. 1** (MHS001) from Huami using Upbeat Tech
- **Integrated biometric signal processor** with 4 dedicated AI engines and built-in CNN based inference engine
- **38 percent more efficient** than the Arm Cortex-M4
- Powered by **SiFive E31**



"The world's first artificial intelligence powered wearable chipset"



huami

SiFive

http://3g.donews.com/News/donews_detail/3048636.ht

SiFive Core IP – 101 Design Wins!

Efficient Performance

Scalability

Compelling Feature Set

→

Embedding intelligence for a world of a **Trillion Connected Devices**