Fast Start into RISC-V for AIoT with A+ Core

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Tel Aviv • Munich • Berlin • Tallinn • Paris • London
AloT, What Is It Anyway

- AloT = AI + IoT (Artificial Intelligence + Internet of Things)

- Needed for edge computing
Why Use RISC-V

► RISC-V is an open standard
  • Everyone can use ISA, implement his own core

► Modular yet stable base architecture
  • Compact kernel (I/E)
  • Modular extensions: M, A, C, F, D
    – More on the way: B, J, P, V, S, etc.

► Custom extensibility is the key to advance RISC-V
  • Standardizing on the common baseline
  • Innovating in respective target markets
  • Bridging the legacy

► Supported by world leading enterprises
  • Open Source and Commercial participating

Krste Asanovic¹, Healthy Discussion of Architectural Choices²:

RISC-V was designed to support specialization while avoiding fragmentation by mandating a frozen common ISA standard around which the software community coalesces, while leaving ample space for innovative custom extensions that do not interfere.

Note 1: Chairman of the RISC-V Foundation, Berkeley Professor, and SiFive co-founder
Note 2: EE Times, 7/11/2018
Who Is Andes

► 14-years-old public CPU IP company
► >160 licensees worldwide
► >1Billion Andes-Embedded SoC shipped in 2018

► A founding member of RISC-V Foundation
► A major open source maintainer/contributor
► Actively involved in standard extensions
  • Chair of P-Extension (Packed DSP/SIMD) TG
  • Co-chair of Fast Interrupt TG
Andes V5 Product Overview

Best extensions to RISC-V

AndeStar™ Architecture V5

AndesCore™ Processors
- Highly optimized design with leading PPA

AndesSight™ Tools
- Professional IDE with high code quality

AndeShape™ Platforms
- Handy peripheral IPs to speed up SoC construction

AndeSoft™ Stacks
- Extensive SW stacks from bare metal, RTOS to Linux

Andes Embedded™
- Best extensions to RISC-V
AndeStar™ V5 ISA – Extending RISC-V

► RISC-V Standard Extensions
  • RV32IMAC/EMAC**
  • RV32I/RV64I-MACFDP_N*
  • RV32FD*/RV64FD*: IEEE754 single-/double-precision floating-point

► Andes Performance Extension
► Andes CoDense™ Extension (12% smaller code size (CSiBE))
► Andes Custom Extension™ (ACE)* framework for DSA (Domain-Specific Architecture)
  • Powerful tools to automate housekeeping tasks
  • No need to have CPU background

** : 22-series only
* : 25-series only
Andes RISC-V Roadmap

Next

Cache-Coherent Multicores

Linux with FPU/DSP

Fast/Compact with FPU/DSP

Slim and Efficient

Cores with higher total performance

A25MP
1/2/4 A25, L2$, L1/I/O coherence

AX25MP
1/2/4 AX25, L2$, L1/I/O coherence

A25
N25F, MMU, DSP

AX25
NX25F, MMU, DSP

N25F
V5/32b, FPU, PMP

D25F
N25F, DSP

NX25F
V5/64b, FPU, PMP

N22
V5[e], 32/16 GPR

N25F, MMU, DSP

NX25F, MMU, DSP

32bit
64bit

5-stage
>1.2GHz
3.58 CoreMark
2.09 DMIPS

2-stage
700MHz
3.95 CoreMark
1.80 DMIPS

Taking RISC-V Mainstream
Andes RISC-V 22-Series Core Overview

- **AndeStar V5 architecture:**
  - RV32-IMAC, or RV32-EMAC + Andes Extensions

- **2-stage pipeline, single-issue**

- **Configurable multiplier**

- **Optional branch prediction**

- **Optional I cache and Local Memory**

- **Bus interface**
  - AHB-Lite and optional APB

- **Also available as:**
  - FreeStart Evaluation Program (FSEP)
  - FreeStart Mass-production Program (FSMP)
Andes AE250 Platform Offering

CLIC
Debug
N22
Master

JTAG
System Interrupts

GPIO
PWM/PIT
RTC
QSPI
UART
WDT

AHB-Lite
Bus Matrix

Inst Memory
Data Memory

Bus Masters
Bus Slaves
Sys. Mgmt Unit

CPU Subsystem
AHB IP
Customer’s or partner’s IP
APB IP

Taking RISC-V Mainstream
Andes RISC-V 25-Series Core Overview

- **AndeStar V5 architecture:**
  - RV32/RV64-IMAC + Andes Extensions
  - Optional FPU: SP, DP
  - Optional DSP/SIMD: P
  - Optional S-mode/MMU: SV32/39/48
    - Support all page sizes
  - RV-N: user-level interrupt

- **5-stage pipeline, single-issue**
- **Configurable multiplier**
- **Optional branch prediction**
- **I/D caches and Local Memory**
  - Optional parity or ECC protection
  - Hit-under-miss caches
  - HW unaligned load/store accesses
- **Bus interface**
  - A master port (AHB/AXI)
  - An optional slave port (AHB)
Andes AE350 Platform Offering

25-series BIU

Inst. Memory
Data Memory

CPU Subsystem
AXI/AHB IP
APB IP
Customer’s or Partner’s IP’s

JTAG
Interrupt Requests

JTAG Debug Xport
Debug Module

PLIC

DMA

APB Bridge

AXI/AHB Bus Matrix

Bus Masters
Bus Slaves

GPIO
I2C
PWM/PIT
RTC
QSPI
UART
WDT

Sys. Mgmt Unit
RISC-V P-Extension

- Andes contributed market-proven DSP (SIMD) as P-Extension draft (32/64-bit)

- designed to accelerate slow video, audio/voice and low data rate DSP workloads

- DSP is optimized for low-power and small-area SoC while vector extension uses more area and power for more performance-demanding applications

* 8-bit SIMD on RV32 example
# Speedup with P-extension on 25-Series

- **Real world speedup, using DSP extension**

<table>
<thead>
<tr>
<th></th>
<th>32 bit</th>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RV32P</td>
<td></td>
<td>RV64P</td>
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<tr>
<td>CIFAR10 (Image Classification)</td>
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<td>10.99x</td>
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<td>AMR voice codec</td>
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<td>3.67x</td>
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<td>7.57x</td>
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<td>ML-KWS (Keyword spotting)</td>
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<td>5.36x</td>
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<tr>
<th>Factors</th>
<th>x</th>
<th>2x</th>
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</tr>
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Custom extensibility is the key to advance RISC-V

Andes Custom Extension (ACE) framework for supporting Domain Specific Acceleration
- Andes tool COPILLOT automate adding your custom extensions

![Graph](image_url)
- Inner Product of Vectors with 64 8-bit Data: 85x
- CRC32: 162x
Andes Custom Extension (ACE)

- C code
- Verilog
- Attributes

- scalar/vector
- background
- wide operands

Automated Env. For Cross Checking
Test Case Generator

Extended ISS
Extended RTL

Extended Tools

COPILLOT
Custom-OPtimized Instruction developeLOpment Tools

Extended ISS
CPU ISS (near-cycle accurate)

Extended RTL
CPU RTL

Compiler
Asm/Disasm
Debugger
IDE

Extensible Baseline Components
Andes V5 Product Overview

**AndesCore™**
Highly optimized design with leading PPA

**AndeStar™** Architecture V5

**AndeSight™** Tools
Professional IDE with high code quality

**AndeShape™** Platforms
Handy peripheral IPs to speed up SoC construction

**AndesSoft™** Stacks
Extensive SW stacks from bare metal, RTOS to Linux

**Best extensions to RISC-V**
AndeSight™ – Rich Features GUI Development

AndeSight™ IDE
- Eclipse-Based GUI
- Streamlined GUI
- Feature-rich Editor
- Managed Build System
- Optimized Toolchains
- Source Level Debugger
- Profiling Analysis
- Flash ISP
- Extensive Demo Projects

Build executables
Debug interactively

AndeSoft™ Target SW
- Application Layers
- Middleware
- Generic Drivers
- App Drivers
- OS/Kernel
- Libraries

Virtual SoC Configuration

SoC based on AndesCore™

Profiling/tracing data

Andes/Partners’ solutions
Customers’ Designs

AndeShape™

Taking RISC-V Mainstream
AndeSight™ – Rich Features GUI Development

RTOS Task List

RTOS Event List
Andes Comprehensive Development Tools

► **AndeShape™ Development Boards**
  - Full-Featured ADP-XC7K
  - Compact Corvette-F1 (Arduino-compatible)
    - With 802.15.4 and ICE on board

► **Debugging Hardware**
  - AICE-MINI+, AICE-MICRO

► **Near-Cycle Accurate Simulator**
  - Qemu Virtual Board
    - AX25+AE350 SoC platform, booted U-Boot/Linux
    - openSUSE project used it for UEFI development

► **AndeSoft™ Software Stack**
  - Bare metal demo projects
  - RTOS’es: FreeRTOS, ThreadX, Contiki, more
  - Linux: RV32/RV64, UP and SMP

► **Rich Support from 3rd Parties:**
  - IAR, Imperas, Lauterbach, Segger, UltraSoC, etc.
SEGGER J-Link Probe

- Support Andes RISC-V CPU cores
  - 25 Series
- Easy to use, efficient and reliable debug probe

- Ultrafast 1.88MB/s download speed
- Unlimited breakpoints in flash memory
- Cross-platform support (Windows, Linux, Mac)

J-Link Remote Server with tunnel mode
SEGGER Embedded Studio

Cross-platform IDE – Embedded Studio

- Cross-platform support (Windows, Linux, Mac)
- Highly efficient Runtime Library for reduced RAM and ROM usage
- Professional tools free for non-commercial use and evaluation
- Direct integration for J-Link
- Other debug probes via GDB protocol
- Ultrafast build process
Summary

► AIoT requires devices with computing performance and low power
  • Andes Custom Extension and/or DSP perfect fit to reach this goal
► Andes offers industrial high-quality RISC-V CPU IP
  • Pure-Play Core IP company since 2005
  • Silicon proven, billions of cores shipped through customers’ SoC shipment
  • Leading PPA and Code Density size
  • Advanced and Comprehensive Development Tools
  • Rich SW/Toolchain Expertise
    – Major toolchain maintainer
    – Excellent support capabilities

Andes: Trusted Computing Expert and Your Best RISC-V Partner!
Go for RISC-V with

Thank you!

For more information, please visit our tabletop or www.andestech.com