A RISC-V ISA Extension for Ultra-Low Power IoT Wireless Signal Processing

Carolynn **Bernier**, Hela Belhadj **Amor**, Zdeněk **Přikryl**

Who is Codasip?

- The **leading provider** of RISC-V processor IP
  - Bk series of RISC-V-compliant processors
- Company founded in 2014 in the Czech Republic
- Founding member of the RISC-V Foundation, www.riscv.org
  - Member of several working groups in the Foundation
  - Actively contributing to LLVM and other open-source projects
- Now **Codasip GmbH**
  - Headquarters in Munich, Germany
  - R&D in Brno, Czech Republic
  - Offices in Silicon Valley, US, and Shanghai, Pudong PRC

Who is CEA Leti?

CEA

- The French Alternative Energies and Atomic Energy Commission
- **Most innovative research organization in the world**, Thomson Reuters, 2015
- A key player in research, development and innovation in four main areas:
  1. Defense & security
  2. Low carbon energies
  3. Fundamental research in the physical sciences and life
  4. Technological research for industry
- 20k employees, 1350 PhD and postdoc students
- 704 patent applications in 2018

CEA Leti

- Micro and nanotechnologies research institute of CEA
  - Headquarters in Grenoble, France
  - 65 startups created since foundation in 1967
- Silver member of the RISC-V Foundation, www.riscv.org

Scalable Radio Solutions for Ultra-low Power IoT

- Dozens of standardized IoT standards for **short-range** and **long-range** IoT
- Industrial IoT often requires proprietary IoT protocols
- Extended lifetime of IoT applications (+ 10 year deployments):
  - Industrial IoT requires future-proofed designs
  - Satellite IoT systems require physical layer protocol updates

→ **How to handle it?**

Software-Defined Radio (SDR)

- Many commercial platforms
- Easy to add a new protocol
- Easy to update over time
- And other benefits

But with the GPP CPU it is *not* ultra low power (nor cheap)

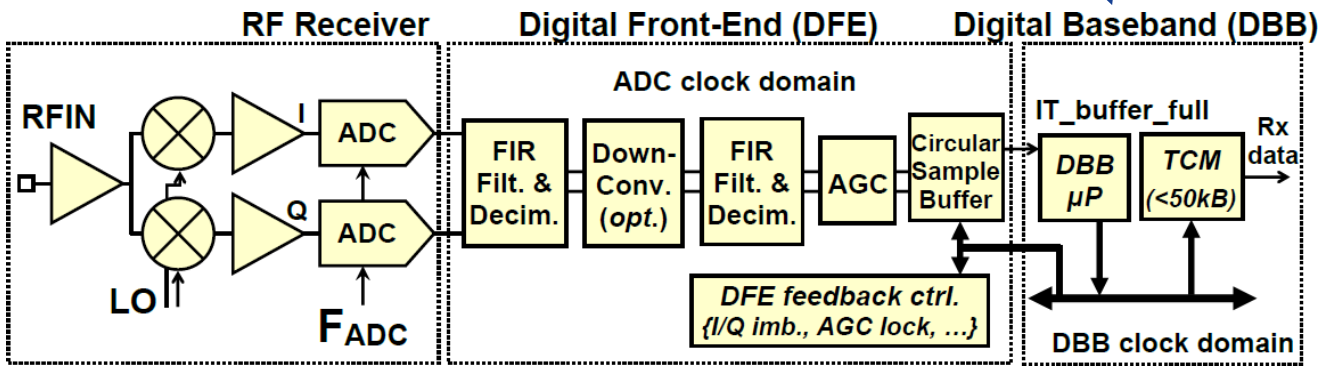
TABLE IX
COMPARISON OF EXISTING SDR PLATFORMS

	Programm-ability	Flex-ability	Port-ability	Modul-arity	Computing Power	Energy Efficiency	Soft Core	FPGA	Cost (USD)
Imagine-based [151]	✓	×	×	×	Medium	Low	Imagine Stream Processor	N/A	N/A
USRP X300 [17]	✓	✓	×	✓	High	Low	PC	Xilinx Kintex-7	$\sim 4-5K$ Total
USRP E310 [17]	✓	✓	✓	✓	High	High	Dual-core ARM Cortex-A9	Xilinx Artix-4	$\sim 3K$ Total
KUAR [34]	✓	×	✓	×	Medium	Low	Pc + 2× PowerPC cores	Xilinx Virtex II Pro	N/A
LimeSDR [146]	✓	✓	×	✓	High	Low	PC	Intel Cyclone IV	~ 300 Board Only
Ziria [147]	✓	✓	×	×	High	Low	PC	Depends on App	N/A
Sora [18]	✓	✓	×	×	High	Low	PC	Xilinx Virtex-5	~ 900 Board Only
SODA [67]	✓	✓	✓	×	High	High	ARM Cortex-M3 + Processing Elements	N/A	N/A
Iris [148]	✓	✓	✓	✓	High	High	Dual-core ARM Cortex-A9	Xilinx Kintex-4	$\sim 1.2K$ Total
Atomix [19]	✓	✓	✓	✓	High	Medium	TI 6670 DSP	N/A	~ 200 DSP Only
BeagleBoard-X15 [159]	✓	✓	✓	✓	High	Medium	2× TI C66x DSPs + 2× ARM Cortex-A15 & 2× M4	N/A	~ 270 Board Only
Airblue [20]	✓	✓	✓	✓	High	High	N/A	Intel Cyclone IV	$\sim 1.3K$ Board Only
WARP v3 [21]	✓	×	✓	✓	High	High	2× Xilinx MicroBlaze cores	Xilinx Virtex-6	$\sim 7K$ Total
PSoC 5LP [164]	✓	×	✓	✓	Low	High	ARM Cortex-M3	N/A	10 Board Only
Zynq-based [166]	✓	✓	✓	✓	High	High	Dual-core ARM Cortex-A9	Xilinx Kintex-4	$\sim 1.2K$ Total

[Akeela, 2018 https://www.sciencedirect.com/science/article/pii/S0140366418302937]

Which CPU for ULP IoT?

- Target architecture is a very small and fast CPU associated with ITCM and DTCM
- Wireless DSP requires linearity and low distortion
  - Operators MUST NOT saturate
  - Operators MUST NOT overflow → but checking for overflows is too costly
- Wireless DSP must conserve dynamic range (DR)
  - The useful signal is often contained in the least significant bits
  - Beware of quantification noise → take care when rescaling the signal
- Most wireless signals are complex : i(t) + j*q(t)
  - Frequent use of MUL, ADD, SUB, MAG, SHIFT, … instructions on 8/16/32 bit complex data
- Demodulation/compensation algorithms are mostly based on correlations → i.e. multiplication
- Input signal stream is typically <= 8 bits
  - Data streams are typically 8 / 16 / 32 bits → fits well on a 32-bit machine
- **Ideal case for RISC-V with ISA Extension**



Exploring the ISA Extension Jungle

Opportunities

- 16 or 32-bit instructions
- Wide opcodes → up to 5 operands
- First operation on 8-bit data is ALWAYS a complex multiplication
- Advanced CMOS allows single-cycle complex operators
- Tiny relative cost of ALU operators

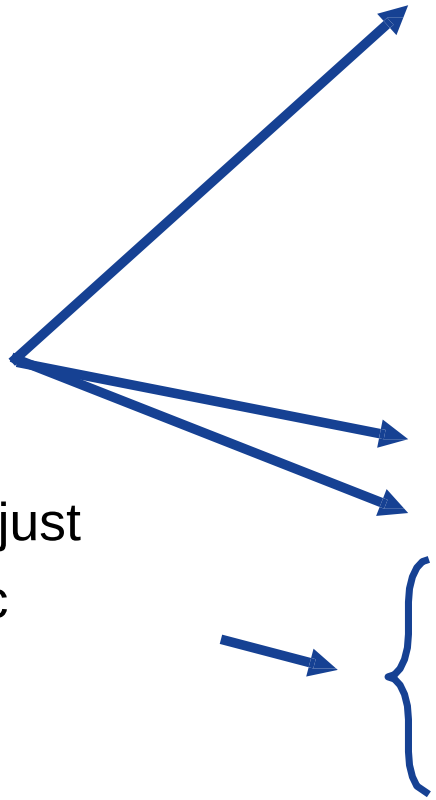
Wanted

- Minimal set of **useful** instructions
- Only 32-bit opcodes for low decoding complexity
- Easy way to explore opportunities, including but not limited to:
  - C compiler
  - RTL
  - Testbench

→ Ideal case for Codasip Bk3 and Codasip Studio

ISA Extension

- ISA exploration done in a few weeks
- Ended with 13 instructions
  - “Zero-cost”
  - Reconfigurable multiplier HW
  - Systematic output dynamic range adjust
  - Efficient automatic gain control

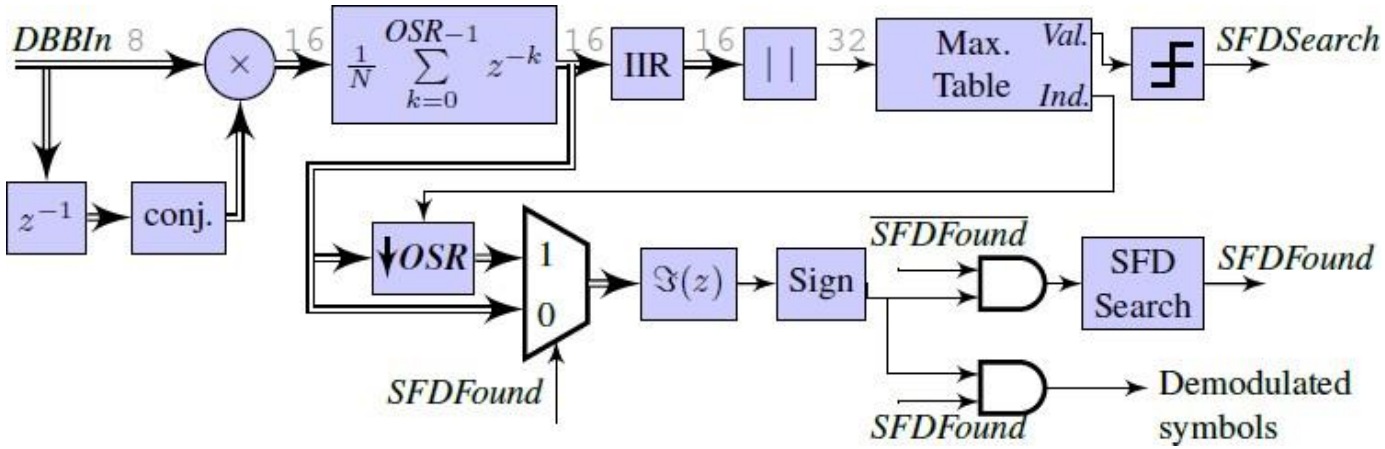


Mnemonic	Instruction
	Zero-Cost Instructions
ADDC16 rd, rs1, rs2, imm	16-bit Addition & Shift Right Arithmetic Immediate
SUBC16 rd, rs1, rs2, imm	16-bit Subtraction
MUL2ADD16-32 rd, rs1, rs2, imm	Two ”16x16” and Signed Addition
SRAC16 rd, rs1, imm	16-bit Shift Right Arithmetic Immediate
SLLC16 rd, rs1, imm	16-bit Shift Left Logical Immediate
CRASC16 rd, rs1, rs2, imm	16-bit Cross Add & Sub
CRSAC16 rd, rs1, rs2, imm	16-bit Cross Sub & Add
MULC8-16 rd, rs1, rs2, H1, H2, C, imm	if C=0: 8-bit complex multiplication, *conj*=1 if C=1: 8-bit complex conjugate multiplication, *conj*=-1
MULC16 rd, rs1, rs2, C	if C=0: 16-bit complex multiplication, *conj*=1 if C=1: 16-bit complex conjugate multiplication, *conj*=-1
MULC16-32 rd1, rd2, rs1, rs2, C	if C=0: 16-bit complex multiplication, *conj*=1 if C=0: 16-bit complex multiplication, *conj*=-1
CLRSB rd, rs	Count leading redundant sign bits
PACK-INIT rs	Initialize packing barrel-shifter
PACK rd, rs1, rs2	Pack a 16 bit complex value on 32 bits after removing *r_sh_pack* redundant sign bits

ISA Extension IoT Testbenches

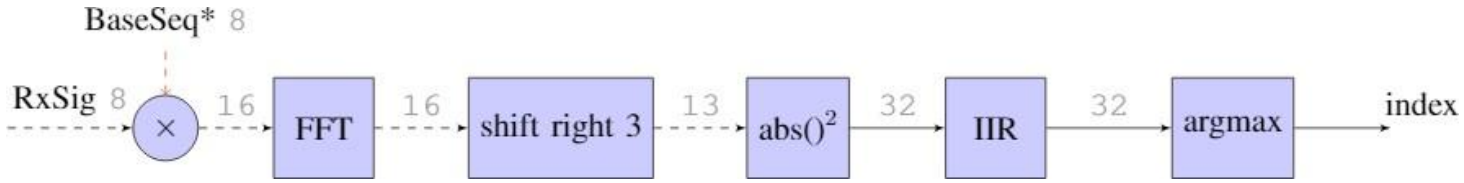
- **Testbench 1**
  - FSK demodulation
  - IoT protocols:

Bluetooth SMART sigfox



- **Testbench 2**
  - LoRa preamble synchronization
  - Spreading Factor (SF) = 7, 11

LoRa



PPA

- Baseline design: **Codasip BK3**, RV32IM
- GF22FDX, 8T, RVT
- Frequency shift key (FSK) Demodulation testbench used for power measurement
  - LLVM flag: -03

	Area	Fmax	Power
Baseline BK3	31.5 kGE	>1 GHz	3.54 µW/MHz
Extended design	40.4 kGE (+ 28 %)	650 MHz (− 35 %)	3.56 µW/MHz (+ 0.5 %)

“Zero” power cost target achieved!

PPA

- Simulation conditions: TT, 0.8 V, 20/24/28, RVT, with clock gating
- Results for the highest complexity phase of algorithm:

IoT Testbench	Baseline			Extended		
	Cycles /sample	Fmin (MHz)	Peak Power (µW)	Cycles /sample	Fmin (MHz)	Peak Power[1] (µW)
Bluetooth LE	68	136	447	51	**102** (− 25 %)	**358** (− 20 %)
LoRa SF[2]=7, BW=125 kHz	164	20.5	135	90	**11** (− 45 %)	**110** (− 19 %)
LoRa SF=7, BW=500 kHz	164	82	303	90	**45** (− 45 %)	**203** (− 33 %)
LoRa SF=11, BW=125 kHz	204	25	149	106	**13** (− 48 %)	**114** (− 22 %)
LoRa SF=11, BW=500 kHz	204	101	357	106	**52** (− 48 %)	**227** (− 37 %)

Ultra-low power target achieved!

Conclusion

- ULP IoT needs SDR
- RISC-V with ISA extension gives the best PPA
- ISA exploration done with **Codasip Bk3** processor and **Codasip Studio**
  - Fast and easy turnaround
  - It’s fun!

PPA clearly shows the benefit of the ISA extension for ULP IoT.

Thank you!

Questions?

www.codasip.com
www.leti-cea.fr