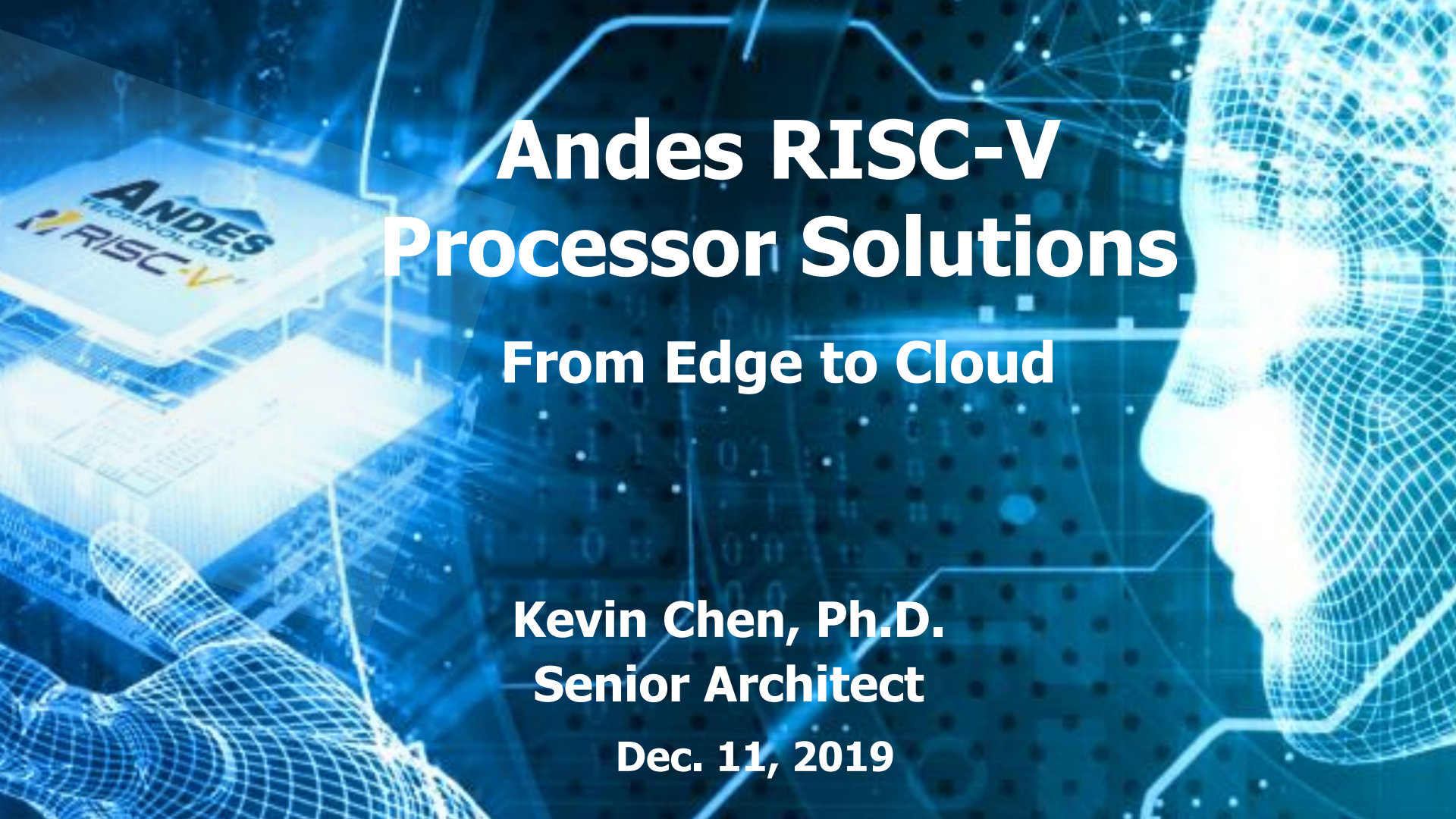

Andes RISC-V Processor Solutions

From Edge to Cloud

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Senior Architect

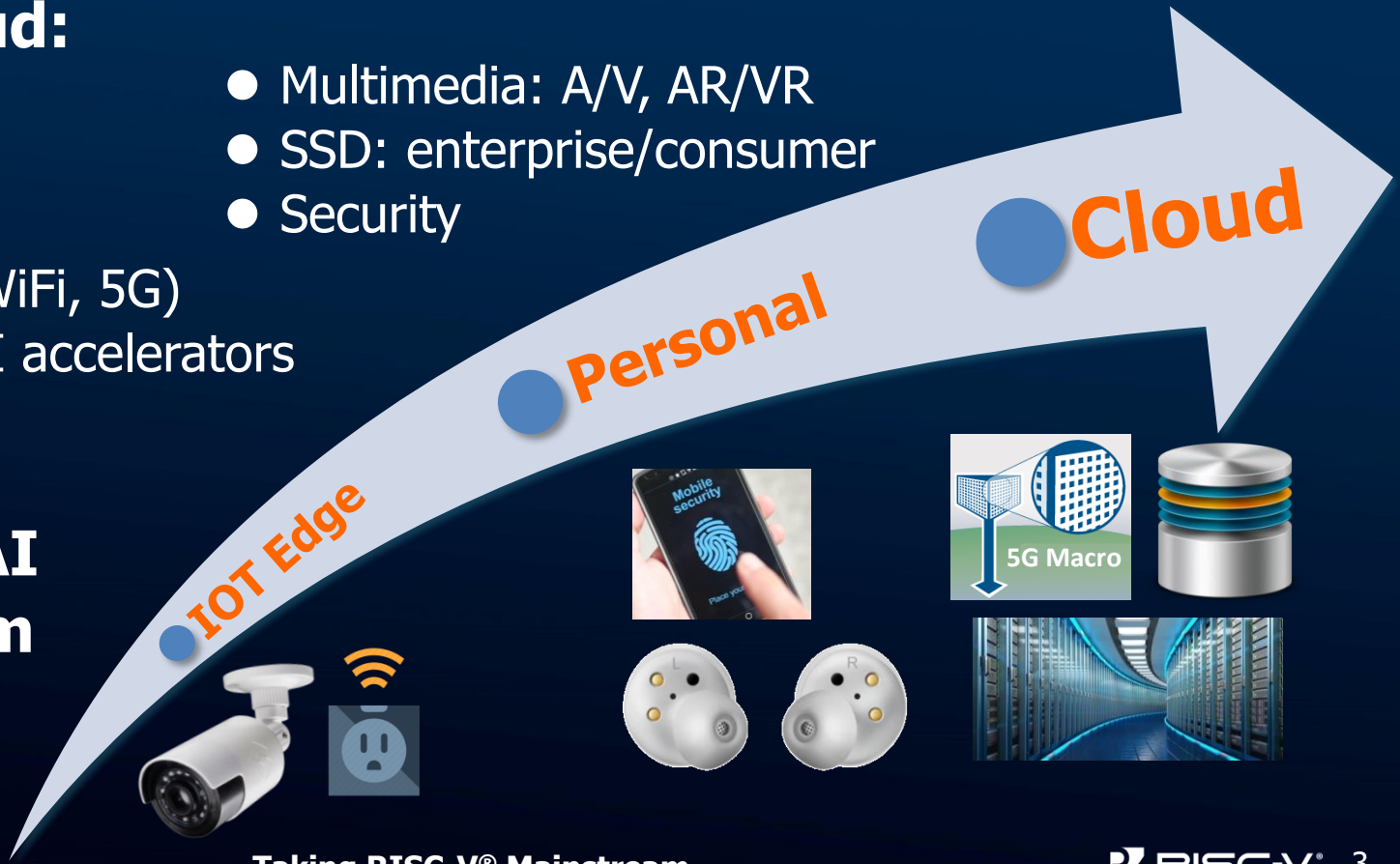
Dec. 11, 2019

Andes Corporate Overview

14-Year Veteran CPU IP Company	• IPO in 2017
>1 Billion Andes-Embedded SoC Chips Per Year	• >180 commercial licensees
Silicon Valley Tie	• Core R&D from AMD, DEC, Intel, MIPS, nVidia, and Sun
RISC-V Founding Member and Major Contributor	• Chairing Task Groups • Contributing to GNU, LLVM, uBoot, glibc, Linux, and more

RISC-V Customers

- **Edge to Cloud:**
  - ADAS
  - AIoT
  - Blockchain
  - Comm. (BT, WiFi, 5G)
  - Datacenter AI accelerators
  - FPGA
  - MCU
  - Multimedia: A/V, AR/VR
  - SSD: enterprise/consumer
  - Security
- **~50% use AI**
- **40nm to 7nm**



Andes RISC-V Processor Lineup

	RV32	RV64
Cache-Coherent 1-4 Cores	A25MP	AX25MP
Linux with FPU/DSP	A25	AX25
Fast/Compact with FPU/DSP	N25F D25F	NX25F

5-stage

Andes RISC-V Processor Lineup

	RV32	RV64	Vector	Superscalar
Cache-Coherent 1-4 Cores	A25MP	AX25MP	27-Series: A/N*27V Vector Ext. MemBoost and more.	45-Series: A/N*45 Superscalar MemBoost and more.
Linux with FPU/DSP	A25	AX25		
Fast/Compact with FPU/DSP	N25F D25F	NX25F		
	5-stage		5-stage	8-stage

Common feature: Andes Custom Extension (ACE)

First RISC-V Cores with RV-P

- **P-Extension ISA for efficient SIMD/DSP (based on GPRs)**

  32= 32 + 8x8 + 8x8 + 8x8 + 8x8

  RV32 performs one set of the above; RV64 performs 2 independent sets

- **Significant speedups on audio:**
  - MP3 decoder: **2.0**x
  - AMR voice codec: **3.7**x

- **Significant speedups on AI:**
  - Keyword Spotting (Tensorflow model): **5.2**x
  - Image classification (CIFAR10): **14**x
  - Face detection (P-net): **8.9**x

Create Your Own Instructions with ACE

Items	Description	
Operands	**standard**	immediate, GPR, baseline memory (thru CPU)
	custom	• ACR, ACM, ACP (ACE Register, Memory, Port) -- With an arbitrary width and number • ACR operands can be "implied" to save opcode
Instructions	**scalar**	single-cycle, or multi-cycle
	vector	**for** loop, or **do-while** loop
	background option	retire immediately, and continue execution in the background. Applicable to scalar and vector.
Auto Generation	- Opcode assignment: automatic based on bits required for operands - All required tools, and simulator (C or SystemC) - **RTL code for instruction decoding, operand mapping, dependence checking, input accesses, output updates** - Waveform control file	

ARM's recent offering

Thanks ARM for finally recognizing the importance. But, it's too little.

Thank You !