SHAKTI Processor Project

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Processor IPs

E-class

3-stage

C-class

5-stage

I-class*

12-stage

Bluespec System Verilog (BSV)

* Work in progress

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Processor IPs

E-Class

Features:

- 3-stage in-order
- ISA: RV[32/64] I [ACM]
- Can boot FreeRTOS, Zephyr

Src: https://gitlab.com/shaktiproject/cores/e-class

Artix-7 FPGA

Config	RV32IACM	RV64IACM
LUTs	2.5K	3K
Clock freq.	100 MHz	100 MHz

180nm ASIC

Config	RV32IACM	RV64IACM
Instances	22.6K	40.7K
Clock freq.	100 MHz	100 MHz

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Processor IPs

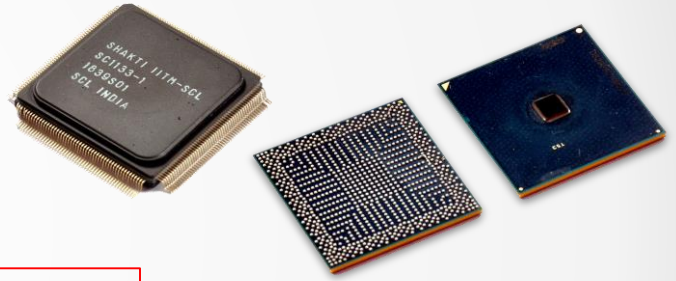
C-Class

Features:

- 5-stage in-order
- ISA: RV[32/64] I [ACFDMNSU]
- Branch predictor + RAS
- Daisy-chained CSRs
- 1.72 DMIPS/MHz
- Can boot Linux kernel

Prototypes

180nm | 22nm (LP)



Src: https://gitlab.com/shaktiproject/cores/c-class

Artix-7 FPGA

	RV32IACMNSU	RV64IACMNSU
LUTs	4.5K	6.5K
Clock freq.	100 MHz	80 MHz

65nm ASIC (LP)

	RV32IACMNSU	RV64IACMNSU
Instances	40.2K	80K
Clock freq.	400 MHz	340 MHz

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Core Configuration

ISA

RV[32/64]I[ACFDM], Supervisor and User support, User-trap support

Caches

Sets, Ways, Banks, Fill buffer size, ECC, TIMs

Branch Predictors

History Size, BHT and BTB Sizes, RAS Size

MMU support

Supervisor mode support, TLB Sizes, ASID width

Misc

PMP Size, Triggers, Debug support, Performance counters

Simulation

Verilator/VCS/Incisive, Coverage and Trace, Multi-threaded

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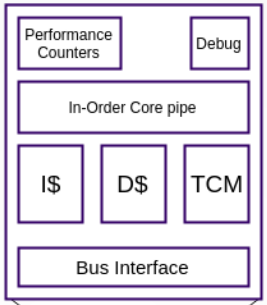
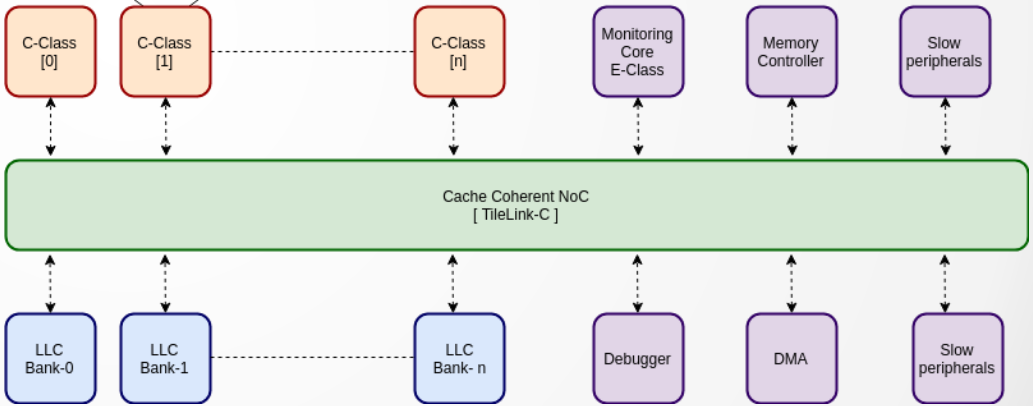
Multicore

- Parameterizable no. of application cores (1-32 cores)
- Directory-based MSI cache coherence
- System management with monitor core
- TileLink-C bus protocol
- NoC with mesh topology

In Collaboration with Thales



SafeRV



Safety critical applications

- Criticality aware NoC
- Triple Lock-Step (TLS) pipeline for fault tolerance*

* Work in progress

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Uncore IPs

- Bus protocols
  - AXI4/AXI4-Lite
  - TileLink-U/H
- Bridges to/from AXI4 and AXI4-Lite with different data bus widths and clocks
- Posit-arithmetic Units + Compiler
- Peripherals
  - SPI
  - Quad SPI
  - I2C
  - DMA
  - PLIC
  - PWM
  - Timers
  - Watchdog
  - UART

* For select FPGAs

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Offerings

Core + Uncore IP

- Various classes of processors
- Bus protocols
- Peripherals
- Fully automated FPGA bitstream generation

Verification

- CoCoTb VIPs: Coroutine Co-simulation Verification IPs*
- AAPG: Automatic Assembly Program Generator
- RiTA: RISC-V Trace Analyzer
- RISCV-Config Legalizer
- RISCOF: Compliance Testing
- RiVer: RISC-V Verification as a plugin infrastructure*

Software

- Integrated Development Environment (IDE)
- Software Development Kit (SDK)
- RISC-V OCaml and Mirage OS*

Research*

- Systolic Array
- Crypto accelerators
- Side-channel attack resistance
- Fat-pointers
- Compartmentalization

* Work in progress

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https://shakti.org.in