

## RISC-V is inevitable

#### Calista Redmond

**CEO RISC-V International** 

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@risc v

March 2024

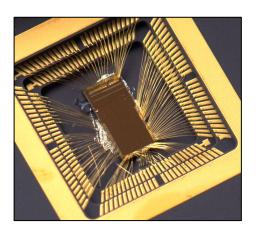
#### Global standards are catalyst to accelerate technical innovation



Standards have been critical to technology innovation, adoption, and growth for decades



Standards create access to opportunities and spur growth for a wide range of stakeholders



RISC-V is a standards-defined Instruction Set Architecture developed by a global community



# The definition of open computing is RISC-V

RISC-V is the most prolific and open Instruction Set Architecture in history

#### RISC-V is inevitable

Mission: RISC-V is the industry standard ISA across computing

- >10 Billion RISC-V cores already shipped
- Adoption moving rapidly across all domains
- Demand at every performance level (low to ludicrous)
- Shared investment driving ecosystem

## RISC-V enables the best processors

RISC-V enables profound innovation from low end to high end applications

- Inherent and sustainable performance and efficiency advantage
- Design flexibility and freedom
- Supported by massive community enabling the most efficient designs for full spectrum of applications
- Modern design for fewer instructions

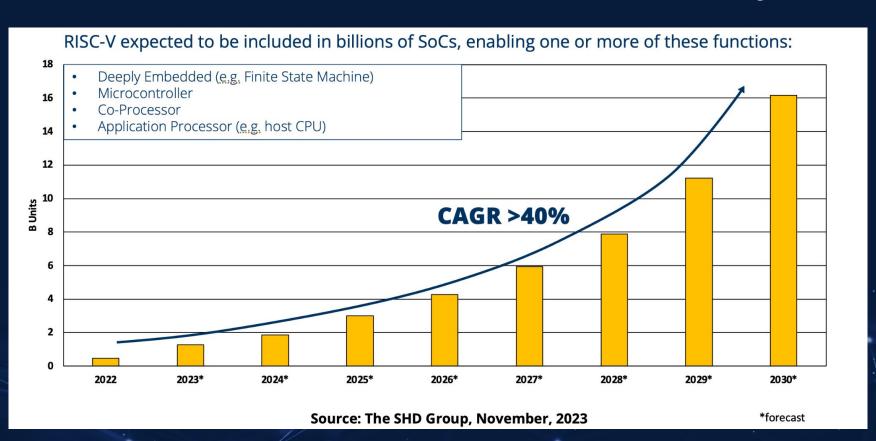
## RISC-V is rapidly building the strongest ecosystem

RISC-V instrumented with software top of mind

- Open standards enable software choice Applications keen to run on RISC-V.
- Toolchain and OS support required for Extension ratification
- Single hypervisor standard to simplify and unify application support
- Thousands of software developers
- Strategic investment by industry and geographies

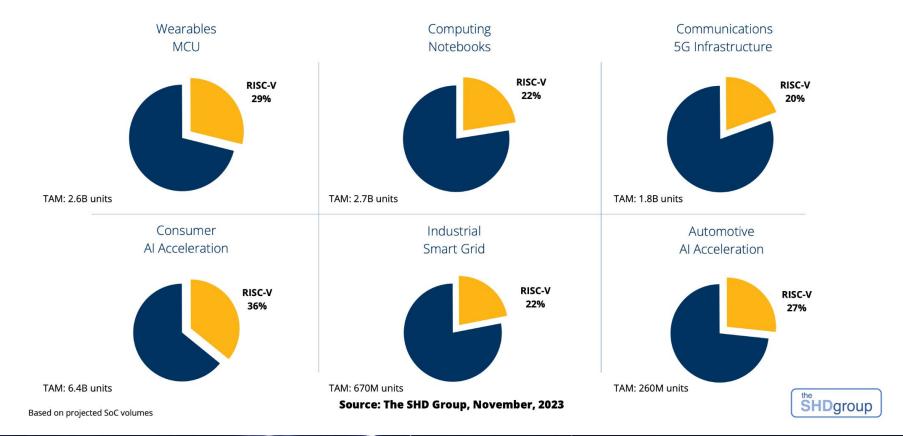


#### RISC-V will be in more than 16 billion SoCs by 2030





#### **Selected Market Share Projections for RISC-V in 2030**





#### **New RISC-V processors**









Codasip first commercial CHERI security implementation

RISC-V Tensor Unit for ultra-fast AI solutions

Performance P870 and Intelligence X390 for generative AI and ML Data center CPU chiplet solution with I/O hub, DDR memory, PCIe, up to 192 cores





**CAST** 



NA900 certified compliant ASIL D of ISO 26262 standard

TESIC RISC-V IP passes SERMA CC EAL5+ security tests

BA5x™ RISC-V processors for low power and EMSA5-FS for functional safety Use of AI to design RISC-V CPU in under 5 hours



#### **Applications**

#### Qualcomm

esperanto.ai





Qualcomm RISC-V wearable platform with Google Wear OS First generative AI RISC-V appliance

RISC-V tablet, portable Linux console, and cluster

Vega, the first RISC-V 10 gigabit **Ethernet switch** 









First RISC-V IoT security Towngas Chip has sold over 1,000,000 units

Two self-developed RISC-V communications chips

Andes N25F for performance and low power in enterprise SSD controller, AndesCore™ RISC-V multicore vector processor

MTIA v1: Meta's first generation AI inference accelerator



### **Developers**



Android added RISC-V to list of supported CPU architectures



ASUS IoT Tinker V board based on AndesCore AX45MP



Industrial edge solutions including High Level Synthesis for C/C++, vector SDKs for AI/ML inferencing



Debian GNU/Linux officially Supported on RISC-V architecture



BeagleV Ahead single board computer released



Terapines ZCC toolchain supports Andes RISC-V processors



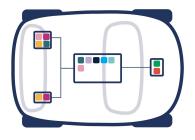
Imperas to Provide Simulation Model of Tenstorrent Ascalon RISC-V Core

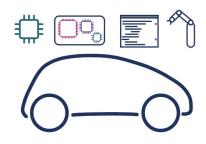


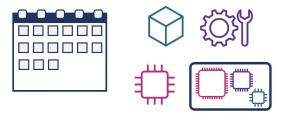
nanoCH32V003 is a 32-bit RISC-V core for \$1.50



### **Industry outlook:** Automotive







RISC-V scales across every compute application in the vehicle

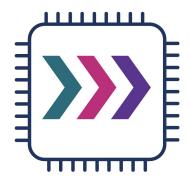
RISC-V enables the supply chain to work together while enabling innovation and differentiation

Ecosystem offers wide breadth of choice, as well as support and expertise required for auto

RISC-V will capture 27% of automotive Al acceleration by 2030



## **Industry outlook: Datacenter & Cloud**



RISC-V offers unique opportunity for accelerators



Custom computing for AI and other emerging workloads

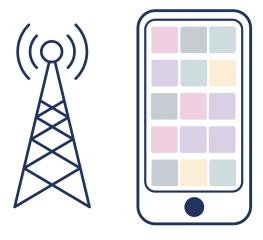


Achieve your performance and power targets

RISC-V CPU core market will grow 115% CAGR, capturing >14% of all CPU cores by 2025



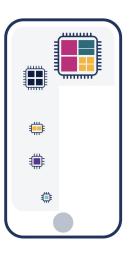
## **Industry outlook: Telecom & Consumer Devices**



Innovation across the industry, from handsets to infrastructure



Android support



Diverse smartphone workloads, from central processing to connectivity to sensors

RISC-V will capture 20% of Communications 5G infrastructure by 2030



## **Industry outlook:** Internet of Things



Streamlined instruction set

enables efficient and compact

and energy efficiency





Strong fit for localized workloads such as machine learning, sensors, and security



Advanced custom processing for workloads like AI to run at the edge

RISC-V will command 28% of the IoT market by 2025 Counterpoint Technology Market Research, September 2021



#### More than 4,100 RISC-V Members across 70 Countries



**121 Chip** Soc, IP, FPGA

3 I/O Memory, network, storage

**23 Services**Fab, design services

**59 Software**Dev tools, firmware, OS

4 Systems

14 Industry Cloud, mobile, HPC, ML, automotive

**165 Research** Universities, Labs, other alliances

**3k+** Individuals
RISC-V engineers and advocates

Dec 2023 update

RISC-V membership up 28% in 2023





# Building the strongest ecosystem

Total market cap of \$5.5T Funding of \$8.5B



landscape.riscv.org

#### **Engage with RISC-V**



Join RISC-V as a member www.riscv.org

#### **Elevate Industry Leadership**

- Deepen expertise in Special Interest Groups
- Show technical and industry leadership
- Leverage Industry Market development
- Engage global reach of RISC-V marketing, media, and social channels

#### **Achieve Business ROI**

- Reduce technical overhead and accelerate roadmap with global open standard
- Reduced strategic risk implicit in collective investment of global stakeholders
- Accelerate sales pipeline with RISC-V support across channels
- Showcase solutions on RISC-V Exchange and Ecosystem Landscape
- Qualify products as RISC-V Compatible<sup>TM</sup>

#### **Build Strategic Network**

- Cultivate partner, supply chain and customer strategic relationships
- Align and leverage global, local and industry networks, alliances, and events
- Amplify visibility online, and at events

#### **Gain Technical Advantage**

- Gain insight and access to technical deliverables in motion
- Infuse your technical directions in specifications
- Accelerate technical knowledge working with domain experts, cultivate and retain talent
- Be part of local developer groups and industry developer networks



# RISC-V is Inevitable This is the open era of computing.





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