RISC-V®

ANNUAL REPORT

2025

www.riscv.org

Contents

CEO Foreword

Andrea Gallo
CEO, RISC-V International

I stepped into the CEO role in May 2025, fully aware that I had big shoes to fill. RISC-V already had a rich history, real momentum in the market, and a deeply engaged community. Year on year, the bar for 'progress' has been set incredibly high. Yet looking back at the past year, I am genuinely proud of how far we have all come.

We welcomed 17 new members spanning embedded, AI, security, automotive, telecoms, software, and more. We also gained automotive semiconductor leader Infineon as a Premier member; its leadership and commitment to RISC-V is already helping us shape the future of RISC-V in automotive.

In fact, when I look at the milestones that have defined progress in 2025, one trend speaks loudest: RISC-V has become a highly valued architecture for both specific workloads and industry verticals. We're focusing on verticals where RISC-V has unique advantages, such as automotive, data center, edge AI, security and space. You will see that pattern throughout this report.

The market data supports this direction. According to the latest analysis from SHD Group, RISC-V is exceeding expectations. It projects that our market penetration will grow from 2.5% in 2021 to 33.7% by 2031: That is a more than tenfold increase in just ten years, driven by focused adoption in the right places.

A big step forward in 2025 was the ecosystem rallying around the RVA23 profile, which we ratified at the end of 2024. RVA23 is a common baseline for RISC-V application processors running operating systems like Linux. It defines a standard set of architectural features so that operating systems, compilers, libraries, and applications all have one clear target to aim at.

This new clarity has enabled organizations to focus their RISC-V development fully on RVA23. It also gives developers a much more predictable environment: if you build for RVA23, you know your software will run across a wide range of compatible hardware.

But of course, for that to happen we need to ensure that drivers and other critical software elements are upstreamed into the main development branches of key open-source projects such as Linux, instead of maintaining outdated separate RISC-V-specific forks. This upstreaming message has been a major priority for us in 2025, and it will remain central in ensuring that RISC-V 'just works' out of the box, removing friction for everyone.

Upstreaming has been a major priority for us in 2025, and it will remain central in ensuring that RISC-V 'just works' out of the box.

A key partner in this journey, and one I have the utmost thanks for, has been the RISC-V Software Ecosystem (RISE) project. RISE is entirely focused on commercial software readiness for RISC-V, and 2025 saw real, tangible results: funding and coordinating critical work on languages like Go and Java, improving continuous integration for major toolchains and distributions, and launching programs to recognize and support the developers who are porting important projects to RISC-V, not to mention their efforts to optimize the support for pytorch, llama.cpp and IREE on RISC-V.

Alongside the technical work, we have also spent time on how we work together as a community. We continue to create opportunities for people to meet, whether that is in deep technical workshops, RISC-V Summits in Europe, China and the United States, or more informal gatherings. The human connections matter. They are how ideas spread, how problems are solved, and how trust is built.

Finally, I want to highlight an important milestone in our journey towards formal international standardization: RISC-V International is now recognized as an ISO/IEC JTC 1 PAS Submitter by the Joint Technical Committee for information technology (JTC1), and we will now work to submit the RISC-V ISA for consideration as an officially recognized ISO standard.

Many organizations develop standards, but international standards have a special status: they are the most widely accepted in the world. Becoming a PAS Submitter is the result of detailed work by our staff and community throughout 2025 to document how we operate, make decisions, and protect the integrity of the ISA. It has helped us improve our operations, our policies, and our ways of working as an organization and with our members.

As a non-profit, we measure our success in the success of our members. Every specification we ratify, every upstream change that lands in a major project, every new deployment in the field comes from the work our members do to bring RISC-V to life. This report is, in many ways, *their* report.

And if 2025 is any indication, the next 15 years of RISC-V will be even more exciting than the first 15. Thank you for any part you have played in this journey; for the energy and passion you bring, and for the trust you place in RISC-V International.

Enjoy the report.

RISC-V at 15: A Brief History

This report comes in the year we celebrate a key milestone: 15 years since UC Berkeley's Krste Asanović and students Andrew Waterman and Yunsup Lee chose to build their own clean-slate ISA over proprietary constraints and aging open alternatives.

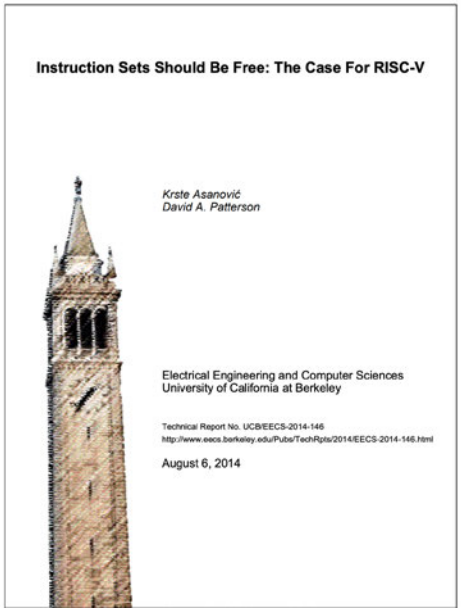
The fifth major RISC ISA (that's *reduced instruction set computer instruction set architecture*) to come out of the university under RISC-founder David Patterson's mentorship, RISC-V was not explicitly designed to be an open architecture, let alone the open standard that it is today. Nor was it expected to grow far beyond academia.

In the first few years, RISC-V was purely a tool for teaching parallel computing design within UC Berkeley's Par Lab. Getting academia outside Berkeley to take note was harder than expected. The fact that it was an open standard wasn't interesting to them. They wanted to teach what the industry was using, and this was just another ISA to have to learn.

The first version of the RISC-V instruction manual was published in May 2011. But it was at the 2014 IEEE Hot Chips 26 Symposium, held August 10-12 2014 in Cupertino, where momentum outside academia truly took off. By the time the team held the first RISC-V workshop in Monterey in January 2015, anticipating a small academic crowd, 40 companies attended.

The Pull of Industry

Fueling the heat that year was a seminal positioning paper published by Asanović and Patterson, titled "*Instruction Sets Should Be Free: The Case For RISC-V*". In it, they doubled down on the open message, likening it to open standards such as TCIP/IP, Ethernet, the C language, and Linux. This comparison helped reposition RISC-V not simply as open hardware, but as a vendor-neutral open standard: something foundational and infrastructure-grade.


Instruction Sets Should Be Free: The Case For RISC-V

Krste Asanović
David A. Patterson

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2014-146
http://www.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-146.html

August 6, 2014

For industry, the paper hit home. Rumble Technologies' Mike Aaronson read it and switched an FPGA-based camera project from MIPS to RISC-V in three weeks. This became the first-ever commercial product to use RISC-V.

At the 4th RISC-V workshop in July 2016, NVIDIA announced plans to replace its proprietary Falcon cores (used for tasks like power management and security inside its GPUs) with RISC-V, driven by a need for 64-bit. This move, which culminated in one billion cores shipped in 2024 alone, may not have grabbed headlines at the time. But it mattered: a top-tier semiconductor company was trusting RISC-V for critical internal functions.

Academia Takes Notice

With RISC-V momentum reaching critical mass, academia finally acknowledged industry demand and embraced RISC-V as the architecture to teach. Institutions globally (including MIT, ETH Zurich, and the University of Bologna) adopted RISC-V in their teaching and research programs.

The time had come to break RISC-V out of Par Lab. So in 2015, the RISC-V Foundation was founded to formalize the ISA as an open standard; rooted in openness, neutrality, and prevent fragmentation. And, of course, to ensure its continued growth, should academia move on to new pastures. In parallel, Asanović, Waterman, and Lee began working on commercializing RISC-V through SiFive. This new company (they imagined) would deliver bespoke silicon for customers, tailored to specific applications. However, this proved far more difficult than had been expected, and after making a handful of customized cores for companies in the embedded space, SIFive pivoted into an IP business.

The founding RISC-V team at the 2014 IEEE Hot Chips 26 Symposium, held August 10-12 2014 in Cupertino CA

From 2015 to 2019, commercial demand began to shift toward production-ready IP. While the ISA's open nature empowered innovation, the burden of functional verification remained a significant barrier to entry and companies began to opt to license proven, pre-verified RISC-V cores from emerging commercial IP vendors.

In 2019, the RISC-V Foundation and the Linux Foundation (LF) announced a joint collaboration agreement to accelerate development and adoption. In 2020, the RISC-V Foundation transitioned into the RISC-V International association, now headquartered in Switzerland. This move reinforced RISC-V's position as a globally governed open standard, independent of any single company or country.

Closing Foundational Gaps

Marketing and leadership initiatives from the early 2020s until now have expanded RISC-V's footprint into new regions and industries, resulting in rapid growth in industry participation and a nascent commercial ecosystem, despite global disruption during the pandemic.

The ratification of the application-level RVA23 profile last year marked another milestone for the architecture. With vector, hypervisor, and cryptology baked in, RVA23 will be crucial in scaling RISC-V into domains such as AI, automotive platforms, and rich operating system (OS) environments such as Linux and Android. Profiles are the foundations of application

and systems software portability across RISC-V implementations, and a large software ecosystem is only possible with a standard profile that software vendors can target, and within which multiple suppliers can work together.

As foundational gaps close, the focus is shifting towards enabling full ecosystems in specific vertical markets, each with distinct needs: software frameworks, toolchains, real-time capabilities, safety standards, and core implementations optimized for different power, performance, and area requirements.

RISC-V in 2025 and Beyond

In 2025, the RISC-V ISA is mature, toolchains stable, and core capabilities robust. We're seeing a global ecosystem where businesses are not only adopting open cores, they're actively building products and creating entirely new markets around them.

What began as an academic exercise has become something far more consequential: shared digital infrastructure for a world that no longer accepts closed, commercial foundations as inevitable. RISC-V's real achievement is not simply technical maturity, but the proof that an instruction set can be governed in the open, evolve collaboratively, and still meet the demands of the most exacting commercial and national-scale deployments.

The combination of a stable ISA, ratified profiles, upstream software, and neutral global governance has turned RISC-V from an alternative into an assumption: a baseline that product teams can confidently build upon for the long term.

As we enter 2026, RISC-V's trajectory looks less like a technology trend and more like a structural shift. The ecosystem now has the ingredients required to sustain itself: credible silicon at every scale, serious software investment, and a growing body of shared engineering that benefits all participants.

In this sense, RISC-V's future is no longer about whether it will succeed, but about how far its model of openness, collaboration, and choice can reach, and how profoundly it will reshape the way computing platforms are built in the decades to come.

The years ahead will see the ecosystem move into a new phase in which performant cores and broader industry confidence enable targeted ecosystem development in industry verticals like space, automotive, data center, embedded, high performance computing (HPC), and security.

This feature appeared in its original, unedited form as High RISC, High Reward: RISC-V at 15 in May 2025.

Industry Momentum

In the 15 years since Andrew, Yunsup, and I founded the RISC-V ISA under the expert guidance of David Patterson, I've delivered a consistent message to audiences at RISC-V Summits around the world:
The State of the Union Is Strong.

Krste Asanović

Chief Architect, RISC-V International

By "union," I refer to the RISC-V ecosystem: its contributors, users, and developers, from multi-national corporations to solo academics, working together under a shared banner to strengthen the standard and deliver real, functioning systems.

For much of the ISA's first decade, "strong" largely meant momentum in establishing RISC-V as a generic, common ISA, supported by foundational software. Compilers, linkers, and toolchains that allowed binaries to run across many devices (the vast majority of those devices being embedded).

Yet even early on, we recognized that RISC-V's long-term success would stem from enabling higher-value, workload-specific systems in markets where one size rarely fits all. From the outset, RISC-V was designed to be modular, allowing innovation in one domain to be reused in another. That reuse, built on a shared base ISA and common software foundations, is one of the main reasons RISC-V has been able to evolve so quickly.

Beyond that common, shared base, each industry vertical requires its own tuned software stack, hardware extensions and ecosystem. Broad adoption requires more than convincing decision-makers that they 'need' RISC-V.

It takes deep, sustained effort to identify gaps, coordinate partners, and implement complete solutions. It's far more important to deliver 100% of what a few verticals need than delivering only 90% of many more.

At RISC-V International, this work happens through special interest groups (SIGs) and task groups. The challenge is not simply building software for a vertical, but doing so in a way that preserves coherence across the broader ecosystem. Leveraging shared components while allowing specialization is what enables sustainable progress.

Much of this momentum has been driven organically by our members. Building on years of work at the silicon, IP, and tools level, RISC-V International and its community have deliberately driven awareness higher up the value chain by engaging OEMs, integrators, and solution providers.

In 2025 we took that effort further, launching targeted campaigns that articulate how RISC-V's unique characteristics address specific challenges in specific vertical markets. As a result, RISC-V is now firmly part of the vocabulary, roadmaps, and procurement choices of decision makers in key sectors.

Today, we're focused on a number of key verticals. In embedded & IoT we already have significant deployment. In data center and automotive, we see ever-growing interest in general-purpose RISC-V compute. Meanwhile, markets that are smaller in socket volume but demanding in capability, such as space and high-performance computing (HPC), are already providing outsized opportunities.

> *In 2025 we launched targeted campaigns that articulate how RISC-V addresses unique challenges in specific vertical markets.*

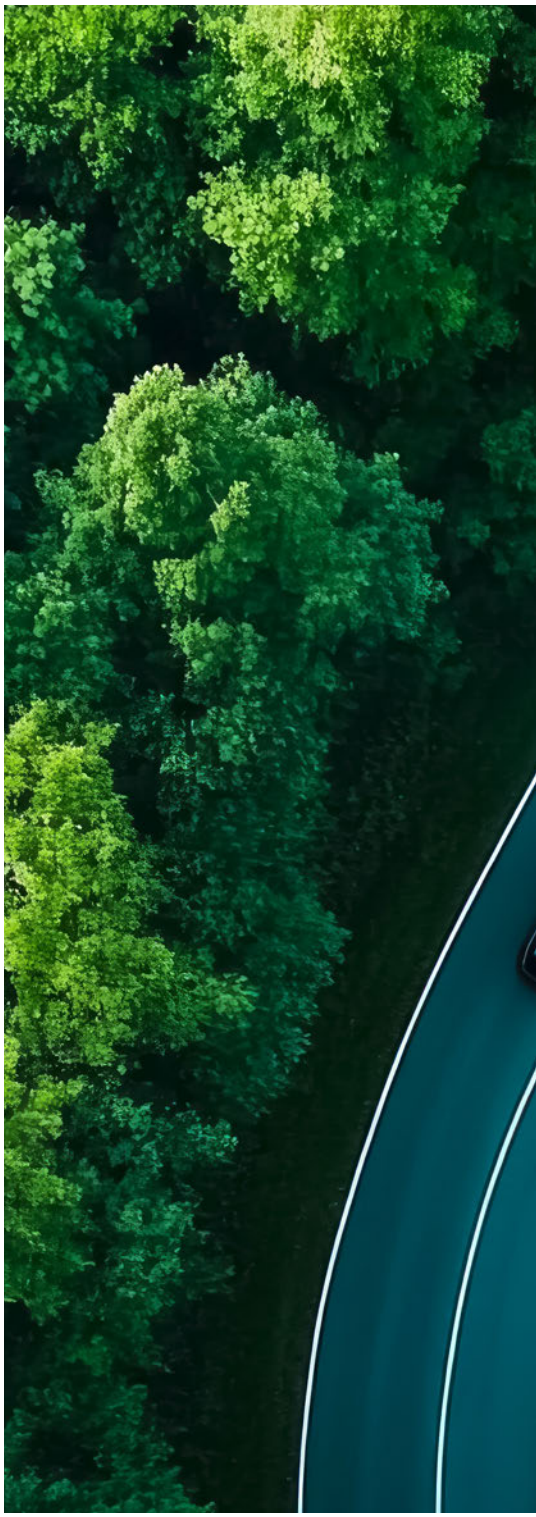
And then, of course, there is AI. Alongside security, AI cuts horizontally across every vertical. There has been a sea change throughout 2025, and it's safe to say that almost every new AI accelerator project I've seen is using RISC-V. This is no accident: we designed RISC-V from the beginning to support scalar, vector, and matrix computation, so it just works. The same cores can handle control and numeric workloads, scale across performance tiers, and evolve with AI.

All the major industry players are starting to recognize that RISC-V will soon be the dominant open ISA. In so many vertical markets, we've moved past *if*. The conversation is now about *how, when* and *where* RISC-V will be adopted.

There is, of course, much to be done. Tuning, libraries, and vertical-specific gaps remain, but the strategy is focused and deliberate. Coherence, reuse, and openness remain RISC-V's greatest strengths. As we enter 2026, the state of the union isn't just strong; it's stronger than ever.

Automotive

The industry remains a vital growth segment for RISC-V, with a strong mix of well-established Tier 1 suppliers and silicon, IP, software and toolchain providers.



This growth is being driven in part by a fundamental transformation in vehicle architectures: moving from traditional domain-based electronic control units (ECUs) toward zonal controller architectures. In zonal designs, physical regions of the vehicle (for example, front left or rear right zones) are managed by smart zonal controllers that consolidate multiple functions and simplify wiring and integration.

RISC-V's scalable, open and customizable ISA enables automotive silicon to be optimized across this range, from real-time local zonal control to centralized compute. This means the same software and tooling can be reused across the vehicle platform.

In March the leading automotive semiconductor manufacturer globally, Infineon, announced that its automotive microcontroller roadmap will be fully based on RISC-V. This move from such a major player in the automotive market demonstrates not only deep industry trust in the maturity of the RISC-V ecosystem, but also a decisive shift toward open, scalable architectures becoming foundational to next-generation automotive systems.

Throughout the past year, the Automotive SIG grew into a very active forum, bringing together automotive domain experts and RISC-V technical experts, combining deep knowledge of functional safety, long lifecycles and regulatory requirements with expertise in ISA extensions, real time, and security.

To sustain this growth, technical work has been ongoing across RISC-V member SIGs to define a standard MCU (microcontroller unit) profile and progress standards on Functional Safety (FuSa), both being fundamental to deliver market-acceptable solutions.

Elsewhere, members with an interest in the segment collaborated to author and publish a whitepaper highlighting the deployment of AI technology in automotive use cases and how RISC-V is specifically suited to handling those workloads.

Data Center

2025 saw the introduction of the first RISC-V based cloud instances by Scaleway and in turn, RISC-V hosting services being offered to public users.

In parallel, important foundational building blocks were put in place to make RISC-V a credible option for servers in mainstream data center environments. In efforts to accelerate adoption, work has been ongoing to ratify specifications for a segment that strongly favors standardization across hardware and software platforms.

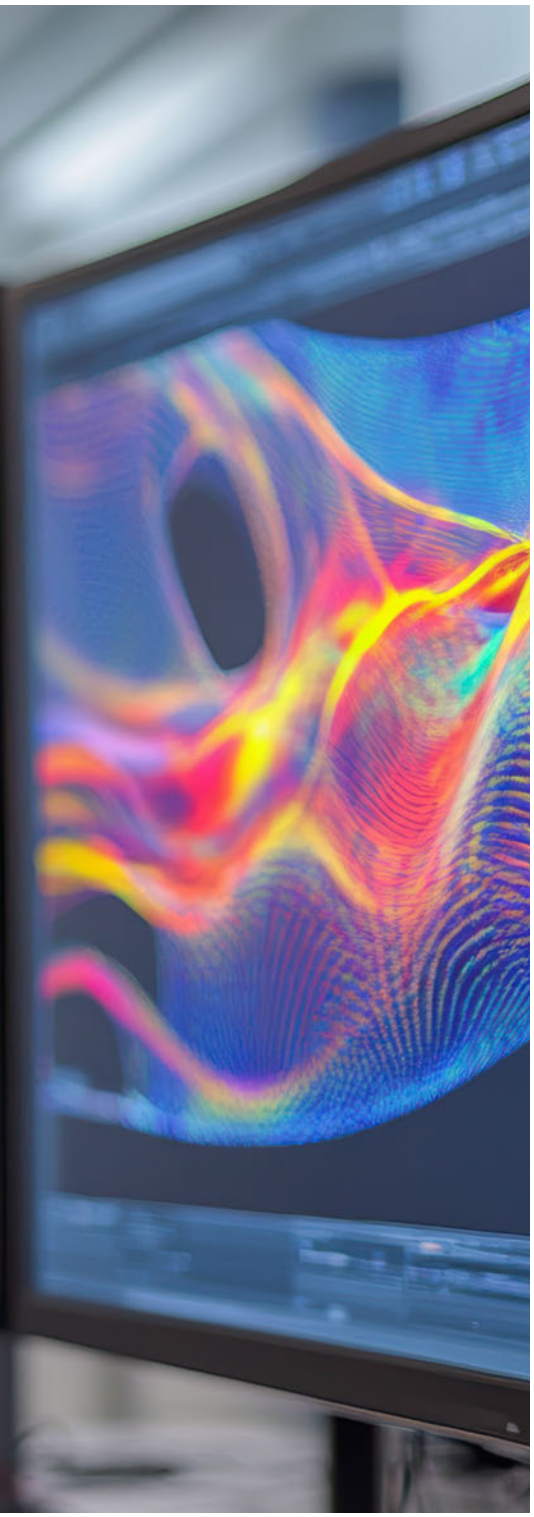
In this respect the Server SoC and Boot requirements specifications have now been ratified and, by the end of 2026, the long-anticipated RISC-V Server Platform specification is expected to be officially ratified.

Alongside RVA23, this will define a standardized set of hardware and firmware requirements (covering unified boot architecture, memory management, interconnects, runtime service etc.) for RISC-V servers, ensuring that high-end RISC-V systems can run enterprise OSes and software out-of-the-box with consistent behavior.

In May 2025 UEFI published ACPI 6.6, the latest version of the Advanced Configuration and Power Interface (ACPI) specification, which for the first time includes native RISC-V support. This makes it easier for data center operators to deploy RISC-V hardware by allowing RISC-V servers to plug into the same firmware and operating system ecosystem already used elsewhere in the data center, reducing risk for adopters and simplifying deployment and management.

New hardware based on the RVA23 profile is expected to be available for data center applications in 2026. RVA23 provides a clear architectural baseline for RISC-V application processors targeting demanding workloads, while still allowing custom extensions for domain-specific acceleration.

In anticipation of its arrival, Linux vendors such as Canonical announced that they are now only targeting RVA23-compatible builds.



High Performance Computing (HPC)

While data center deployments are generally cloud-focused, HPC refers to massive scientific and engineering infrastructures. RISC-V continues to break ground in HPC through initial pilot programs.

Much of the accelerator technology used in HPC has been primarily designed for AI workloads. During 2025 a number of our members introduced RISC-V based accelerators that can be optimized for HPC-specific applications, improving performance and efficiency.

NVIDIA's 2025 announcement that it is porting its CUDA software stack to RISC-V (a development catalyzed by the ratification of the RVA23 profile) signaled strengthened momentum in HPC and AI. The ISA's combination of standardization and flexibility is particularly attractive for HPC users needing the ability to customize the ISA through extensions for HPC-specific application workloads, balancing raw performance with energy efficiency.

In the interim, efforts have been made to ensure the segment is ready when RVA23 hardware arrives. The RISC-V HPC Special Interest Group (SIG) estimates that around a third of the runtime for supercomputers are for applications that have now been ported to RISC-V.

RISC-V also featured prominently in European initiatives aimed at strengthening digital sovereignty in supercomputing. In March, EuroHPC JU formally launched DARE, a large RISC-V-centric HPC/AI initiative coordinated by Barcelona Supercomputing Center, with €120M EU funding plus national co-funding. The aim is to build a RISC-V-based HPC ecosystem, including processors, accelerators and software, under a six-year framework partnership running to 2030.

In parallel, dedicated RISC-V-for-HPC workshops at conferences such as ISC, SC and HiPC brought together application scientists, system architects and toolchain developers to share experience from early RISC-V testbeds and to map out roadmaps for future RISC-V–based clusters.

IoT & Embedded

The Internet of Things (IoT) and embedded markets focus on small, efficient endpoint devices that gather data, control systems, and increasingly perform lightweight AI inference and sensor fusion.

RISC-V based MCUs are already well established with a strong position in this segment. The ability to customize right-sized implementations means that they are perfect for use cases where a defined balance between power, performance, price and area is paramount.

Building upon this momentum, work started in 2025 to define a microcontroller profile that will improve standardization, facilitate reuse and reduce development costs. A draft RVM profile is available now with an expectation that a final version will be ratified in 2026 as the RVM Profile Task Group gains momentum.

As an AI-native ISA, RISC-V enables a balance of scalar, vector, and matrix capabilities. Cores can also simultaneously run the non-AI portion of the application, simplifying software, lowering latency and increasing overall utilization. By running the same AI and non-AI portion of the software on one processor, RISC-V removes memory copies and avoids transfers of data and weights to the AI side, which directly translates to reduced power consumption.

Alongside the ratification of the RVA23 profile for application-class processors at the end of 2024 came the ratification of RVB23, giving IoT and embedded software developers a solid hardware target at which to aim.

Supporting this, RISC-V International announced a collaborative partnership with the Edge AI Foundation at RISC-V Summit North America 2025, bringing together a global community of companies and academics working at the cutting edge of AI, venture capital firms investing in the space, and startups with novel approaches to enabling AI at the edge. The collaboration reflects a shared belief that technologies only transform industries when communities adopt them, evolve them and apply them in the real world, and that building vibrant global communities around RISC-V and edge AI is essential to unlocking this value.


Payload & Flight Data
Payload Mass: 7,200 kg
Fairing Status: SECURE
Satelite: COMM SAT-32
Target Orbit: 450 km - Circular
Flight Parameters
Launch Time: T-00:02:15
Propellant Load: 98.7%
Engine Pressure: 3,560 psi
Guidance Mode: AUTO
Winds: 5.2 m/s NE
System Status: GREEN
Fuel Tanks
Engine Status
Range Safety
FULL 18%
READY
ARMED
Launch Camera
T-00:02:15
LC: GO FOR LAUNCH
Range: GREEN
Weather: CLEAR
Altitude
Speed
G-Force
Pitch: 90.0°
Max Q: 220.5 kPa
Engine Temp: 84°C
AUTOLAUNCH: ENABLED
Tracking: NOMINAL
Telemetry Link: GOOD
ABORT
ARM
IGNITION
DC-ROMA

Space

Space computing is no longer theoretical for RISC-V, with new radiation-hardened IP and member-hosted events in 2025 demonstrating how RISC-V can scale from satellite telemetry to mission-critical, deep-space functions.

This growing momentum is being reinforced by RISC-V's unique drivers, from digital sovereignty to supply chain resilience. Space programs are placing ever-greater value on an open standard ISA that can be sourced, implemented, and supported across multiple vendors and geographies, reducing dependency risk while strengthening long-term program control. In this context, RISC-V is rapidly emerging as the leading ISA for the space market, with the first RISC-V In Space conference taking place in Sweden in April 2025, hosted by the European space agency (ESA) and Frontgrade Gaisler.

A switch in space mission philosophy from long-term government-led projects to multiple short scale public/private sector partnerships also favored RISC-V's Agile open and collaborative development approach. On a technology level, RISC-V's customizable ISA uniquely allows developers to balance Space specific requirements including AI capabilities, fault tolerance, security and efficiency on a single platform that scales across use cases from ground based HPC to onboard processing.

Both NASA and the European Space Agency (ESA) have been in the process of transitioning from obsolete processors and embracing RISC-V based solutions. Back in January, NASA provided an update on its High Performance Spaceflight Computing (HPSC) SoC, built in partnership with Microchip and based on a fault-tolerant, radiation-hard 10-core heterogeneous RISC-V architecture from SiFive.

Space is brutal for silicon: cosmic radiation and EMI can upset delicate electronics by flipping bits in registers, flip-flops, and memory. Frontgrade Gaisler's space-bound and radiation-hardened NOEL-V CPU IP core completed verification in late 2025, validated with advanced tools from Breker Systems.

While space currently remains an emerging market, the impact of new lower cost launch technology is expected to accelerate rapid growth. Furthermore, space technology can be applied to multiple adjacent markets with similar needs for safe, secure, and efficient processors that operate in harsh and hard-to-access environments.

Horizontal Progress

Every breakthrough in a specific vertical market relies on shared horizontal technologies that cut across industries.

Many horizontal technologies contribute, but three do much of the heavy lifting...

- **Artificial Intelligence (AI)** is the intelligence layer, converting data into perception and decisions so systems can adapt on the fly.
- **Security** is the trust layer, protecting identities, data, and update paths in connected, software-defined environments.
- **Software** makes adoption practical, delivering toolchains, OS enablement, libraries, and upstream integration, accelerated through our partners in RISE (the RISC-V Software Ecosystem).

These three horizontals underpin every vertical and are fundamental to RISC-V's overall success. Let's take a look at the progress made in 2025...

Artificial Intelligence (AI)

AI continued to be the defining force behind industry progress across all verticals, with analysis from research company Omdia estimating that global AI processor revenue will increase by almost 50% in the next five years.

Around one quarter of this total, says Omdia, will come from edge AI: devices ranging from tiny IoT endpoints to edge gateways that perform AI computation locally, closer to where data is generated. This is rapidly emerging as one of the most important cross-cutting opportunities for RISC-V.

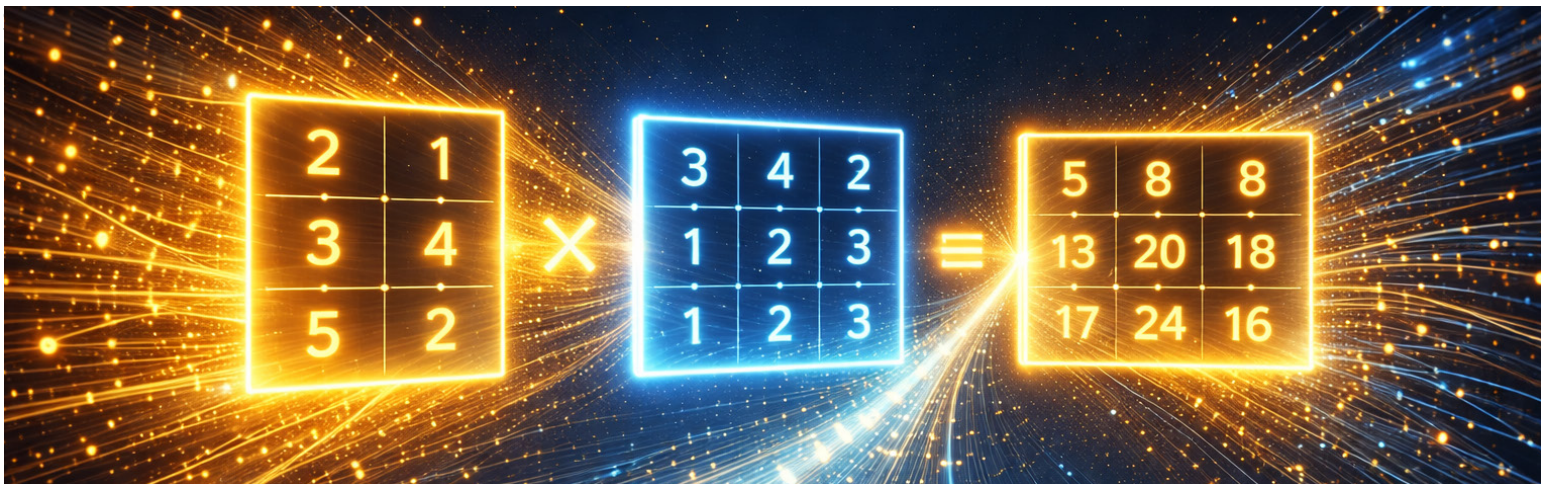
This trend aligns closely with developments in the RISC-V ecosystem. Notably, Google open-sourced its Coral (previously Kelvin) neural processing unit (NPU) in October, offering a full-stack, always-on, low-power edge AI platform built on RISC-V and positioned as a reference design for the wider industry. The processor is now broadly available and has been integrated into Astra SL2610 IoT edge-AI SoCs from Synaptics.

Through the Open Compute Project, cloud and hyperscale players including Google, Microsoft, AMD and others have also standardized on Caliptra, an open, RISC-V-based root-of-trust (RoT) IP block intended to ship in future CPUs, GPUs and SSDs across their fleets.

A major milestone was NVIDIA's announcement that it is adding RISC-V support to its CUDA software platform. By pairing a powerful GPU with a RISC-V host processor, developers can orchestrate GPU-accelerated workloads.

In an interview with RISC-V International, NVIDIA's VP Multimedia Architecture, Frans Sijstermans, explained that the ratification of the RVA23 profile was the catalyst for NVIDIA's decision to bring CUDA to RISC-V. "We wouldn't have considered this without RVA23", he told us. "It didn't just give us a stable hardware target – it gave us the reassurance we'd been waiting for."

Ongoing Work in Matrix Computation



compute, security, platform management, and performance tooling. Of these areas, standardized matrix computation capability stands out as integral to RISC-V's AI strategy in 2025.

The *V* in RISC-V is not only a Roman numeral five (in reference to the fifth RISC architecture to come out of UC Berkeley); it also nods to vectors, reflecting Krste Asanović's long-standing vision for vector processing as a core capability of the ISA. This intent later materialized in the official RISC-V Vector extension (RVV 1.0), a key differentiator for RISC-V compared to other ISAs. RVV provides scalable, flexible vector capabilities aimed at enabling AI in everything from edge devices to HPC.

Matrix computation takes this AI computation capabilities further; while vector operations involve linear arrays, matrix math operates on two-dimensional grids of numbers. A matrix multiply takes two 2D arrays and combines them into a third, and this operation is at the heart of neural networks, signal processing and many HPC workloads.

Nearly every step in a modern AI model, from convolutions in vision to attention in transformers, can be reduced to sets of matrix multiplies. From edge devices doing real-time perception and sensor fusion through to large-scale training and inference runs in the cloud, the AI experiences end-users see (smarter cameras, safer vehicles, more relevant recommendations, more capable language models) all rely on hardware that can sustain enormous volumes of matrix computation efficiently.

Today, RVV1.0 is widely implemented in commercial cores, and a number of AI-focused RISC-V products already enable matrix-based AI acceleration through vendor-specific matrix engines and custom extensions.

Three Routes to Matrix

The next step is to also standardize matrix at an ISA level, a task the community is currently approaching via three pathways:

The **Integrated Matrix Extension (IME)** reuses existing RVV vector registers to store matrices and perform multiplies directly out of the vector register file. This route offers matrix acceleration without the need to add a new architectural state, which means simpler design, reduced die size and power consumption, making it a good fit for embedded and application-class cores that already implement RVV.

The **Vector Matrix Extension (VME)** sits very close to RVV: it takes two vectors, computes their outer product, and accumulates the result into a dedicated matrix accumulator. That outer-product formulation gives high compute density and power efficiency with a relatively small ISA footprint.

The **Attached Matrix Extension (AME)** defines a separate "tile" register file and a richer set of matrix operations: matrix–matrix, vector–matrix, scalar–matrix arithmetic, convolutions, permutations and sparse compression, with its own load/store path. This scales from small embedded AI engines to large HPC-class systems, and can even be used without RVV at all, making it attractive for low-cost AI accelerators that still want a standard RISC-V programming model.

Each approach to matrix calculation demonstrates clear strengths at different implementation points and for different workloads, from edge to cloud.

Going into 2026, the priority is to converge on a standardized set of matrix capabilities that span the full range of RISC-V AI deployments, with clear recommendations for their selection based on target application. Software integration in the same place, e.g. IREE or TVM, will ensure a common approach at the AI/ML stack level.

Security

The last few decades have shown that insecure devices don't just fail quietly; they become part of a far greater problem. Side-channel attacks, remote code execution bugs, hard-coded credentials and weak device management have all contributed to botnets, data breaches and outages that affected millions of users.

In this environment, security in both hardware and software is a decisive factor in whether a platform can be trusted. RISC-V International is prioritizing security across the architecture, standardizing mechanisms that let implementers build systems that are "secure by design" and resilient against the kinds of exploits that have plagued previous generations of technology.

In August, RISC-V International and its members published a white paper describing both ISA-defined and non-ISA mechanisms that enable the instantiation and management of isolated supervisor domains and contexts. In practical terms, it shows how to use RISC-V in a unified way to build secure systems: segmenting workloads, managing isolation and leveraging the modular ISA to implement robust security architectures. This work is relevant not only to security experts, but to anyone seeking to understand how RISC-V can underpin trustworthy systems, from small embedded devices through to large-scale infrastructure.

Unifying Security Under One Coordinating Committee

During 2025, the RISC-V Security Horizontal Committee (HC) matured as the coordination point for much of this work. Several Task Groups (TGs) and Special Interest Groups (SIGs) were streamlined into the HC to simplify their structure and bring them into closer alignment with RISC-V International policies.

The Security HC now connects the Security Incident Response Team, the Security Model Task Group, and the Crypto SIG (redesignated from a TG and now incorporating two managed TGs, High Assurance Cryptography and Post-Quantum Cryptography), and has absorbed the Control Flow Integrity SIG and the microarchitectural side-channel work.

Two other long-standing efforts, being the Security Model itself and the RISC-V Worlds abstraction, also made solid progress in 2025. The Security Model has been reformatted in line with Architectural Review Committee (ARC) comments and will be resubmitted shortly, while RISC-V Worlds is now one of the committee's major

priorities, with current progress indicating that agreement and completion are close. Taken together, this structure gives the community a clearer place to collaborate on security topics and helps align work across profiles and verticals.

A major focus area in 2025 was isolation and confidential computing. The Supervisor Domains privileged ISA and non-ISA extension specification completed ARC feedback, and an initial QEMU-based prototype was created, with Architectural Compliance Test (ACT) work ongoing.

Building on this foundation, academic and industrial projects such as Keystone, IBM's Assured Confidential Execution (ACE), and the Confidential VM Extension (CoVE) explored how to build trusted execution environments (TEEs) and confidential computing on standard RISC-V hardware. CoVE and CoVE-IO completed internal reviews and are now progressing through community feedback towards freeze. A companion application note, Implementing Application Processor TEEs using RISC-V Supervisor Domains, was released to the community.

Together, these efforts provide both the conceptual model and the practical tools needed to deploy TEEs on RISC-V, and the TGs are now focused on ratifying the relevant specifications and transitioning them to broader public review and open-source development.

Establishing Root of Trust

Root of trust (RoT) formed a second pillar of the 2025 security story. RISC-V–based silicon root-of-trust IP Caliptra continued to gain traction as a common, open building block for future CPUs, GPUs and accelerators.

Originally defined in the Open Compute Project and now hosted as an open-source RTL implementation under the CHIPS Alliance, Caliptra provides identity, measured boot and attestation capabilities inside the SoC itself, giving datacenter and device vendors a shared, auditable foundation for consistent, verifiable security at the silicon level. At the OCP Global Summit in October 2025, partners introduced Caliptra 2.1 as a full RoT security subsystem, adding quantum-resilient cryptography and enhanced hardware key-management features aimed at cloud and AI infrastructure.

Alongside Caliptra, open roots of trust such as OpenTitan also moved from prototypes towards broad deployment in 2025. OpenTitan is an open-source silicon root-of-trust design stewarded by lowRISC and its partners, built around Ibex; a hardened, 32-bit RISC-V processor core that runs the root-of-trust firmware and orchestrates secure boot, key management and attestation.

This makes RISC-V the instruction set at the heart of the security controller itself, even though OpenTitan can be integrated alongside a wide range of host CPUs.

Fabrication of production-quality OpenTitan silicon began in early 2025, with Nuvoton preparing volume shipments and Google and other partners planning deployments in Chromebooks and datacenter platforms, underscoring that open, RISC-V–based RoTs are now moving from evaluation boards into real products.

Memory protection and hardware isolation mechanisms also moved forward. The upcoming IOPMP (I/O Physical Memory Protection) specification has been updated to simplify and restructure the document, and there is now renewed optimism that it can progress. SPMP (Supervisor-mode Physical Memory Protection) is in the "editorial comments" stage, so it is expected to move quickly to ratification, alongside the fast-track hypervisor addition, HPMP. In parallel, work on Hardware Fault Isolation (a relatively simple intra–address-space isolation mechanism for user-mode protection) is scheduled to restart next year, complementing the more heavyweight supervisor-domain and confidential-computing mechanisms.

Hardware's CHERI On Top of Secure Hardware

2025 also saw growing interest in hardware-enforced memory safety. The release of the CHERIoT 1.0 specification was a key milestone, and CHERI (Capability Hardware Enhanced RISC Instructions) and CHERIoT-based RISC-V cores, backed by new public investment, demonstrate how capability-based architectures can prevent large classes of memory-safety vulnerabilities and enable fine-grained compartmentalisation in microcontrollers and higher-performance systems.

It is encouraging to see the growing level of industry interest in CHERI, reinforced by new funding rounds and government programmes: most notably the UK's *Digital Security by Design* initiative. In November 2025 a £21 million funding package was announced that includes support for SCI Semiconductor to adopt the higher-performance CHERIoT Kudu RISC-V core in next-generation microcontroller products, signalling a clear path from research platforms to widely deployed silicon.

Looking ahead, microarchitectural side channels and fine-grained isolation continue to be active areas of work within the Security HC. Side channels are being addressed through the Speculation Barriers Task Group, and a new approach is under discussion for temporal fencing. With the release of memory tagging technology on mainstream devices, the RISC-V Memory Tagging TG has also made visible progress, with its specification reaching the internal review stage. The long-recognized need for lightweight isolation beyond RISC-V Worlds has been another focus of the HC in recent months, with the aim to address any identified gaps in 2026.

These developments show RISC-V evolving from isolated implementations to a far more holistic security story, with shared components, common models and a deep research pipeline to draw from.

Software by RISE

It's an age-old 'chicken-and-egg' problem: Modern hardware cannot function without software, yet many of the most important low-level software investments are hard to justify until there's already meaningful hardware adoption.

The RISC-V Software Ecosystem (RISE) Project exists to help break that cycle by pooling engineering effort and funding to move critical open-source software upstream. This enables hardware and software to evolve in parallel and RISC-V application processors can ship into mainstream markets with production expectations around performance and reliability.

Organized under Linux Foundation Europe, RISE provides a neutral home for collaboration while working in close partnership with RISC-V International. RISC-V International focuses on the ISA and its long-term stability, while RISE concentrates on the software that enables RISC-V hardware to be a usable platform for developers and product teams.

In practice, this means an "upstream-first" approach across the whole stack: the developer toolchain, the Linux boot-to-OS path (including distro enablement), virtualization, and the runtime/application layers on top.

Launched in May 2023 by a coalition of major ecosystem players (including Google, Intel, NXP, NVIDIA, Red Hat, Samsung, and Qualcomm), RISE has scaled its impact through member engineering contributions and targeted contracting, alongside broader ecosystem investment to accelerate key software work where expertise or bandwidth is constrained.

Primarily, RISE members participate through member-supported working groups. They contribute to a wide variety of projects, from toolchains and firmware to application stacks, runtimes and system libraries; wherever the broader RISC-V community needs support.

Contributions take the form of direct engineering work by members, sponsored consulting delivered through a structured RFP process, and recognition of existing work through the Developer Appreciation program.

In 2025, RISE's work translated into concrete ecosystem-building steps, particularly in areas that matter for real-world productization. These initiatives have helped narrow long-standing gaps in toolchain maturity and application language support, meaningfully moving RISC-V closer to production-grade software readiness for multiple vertical and horizontal markets.

2025–26 Software Progress by RISE at a Glance

RISC-V Optimization Guide

RISE published the RISC-V Optimization Guide at the end of 2024 to help open-source developers and maintainers not only to port software to RISC-V but also to optimize its function to take best advantage of the hardware. Development of the Guide continued throughout 2025. It is a living document, expected to grow and develop along with the software ecosystem.

RISC-V Support in the Yocto Project

In May 2025, RISE and RISC-V International jointly upgraded our participation in the Yocto Project, pairing governance participation (via RISC-V International's Platinum membership) with engineering support from RISE. This moves RISC-V from "unofficial community support" toward formal enablement in a widely used embedded Linux build and test ecosystem.

This brings broader verification coverage, long-term support expectations, and features like SBOM generation and build reproducibility into the default pathway for RISC-V embedded platform teams. In addition, this effort has now secured Yocto Project Compatible status for the meta-riscv OpenEmbedded layer, ensuring broad ecosystem support.

Focus on AI/ML Software Enablement

RISE formed a dedicated AI/ML Working Group in February 2025 to create an organized place for members to collaborate on AI/ML initiatives, and later hosted a 2025 webinar focused on RISC-V's AI/ML progress and the road ahead, helping concentrate ecosystem attention on software enablement pathways as RISC-V AI deployments broaden.

New RFPs in Progress

One of the ways RISE provides resources to the software ecosystem is through an RFP process, by which third parties can contract to be paid to work on RISC-V software. Since it started, RISE has contributed close to €2 million, and continues to do so with ongoing projects.

In 2025, RISE created five new RFP engagements for RISC-V software, covering support for KernelCI, Pytorch, llama.cpp and GGML, IOMMU support in EFI, and OpenSBI support for TEEs. This work will continue throughout 2026, with four additional RFPs in the works already.

Developer Appreciation Program

The RISC-V Developer Appreciation Program began its initial pilot run from October 2024 through March 2025, and has continued throughout 2025 as a permanent program, offering up to €50,000 in rewards across tiers from small CI/enablement additions through substantial ports (e.g., adding a RISC-V backend and updating testing pipelines).

In a fast-moving ecosystem, targeted recognition of smaller contributions helps turn "someone should do it" work into shipped, upstreamed improvements.

Google Gemini Credits

In late 2025, Google graciously donated a huge quantity of Gemini credits for use in developing AI for RISC-V. RISE posted a call for proposals and has awarded up to $50k USD in credits to several individuals.

Board Chair's View

It's been a very positive year for the RISC-V ecosystem, and the community has achieved a great deal. The challenge now is to maintain that momentum into sustained, visible success across the global market in 2026 and beyond.

Lu Dai
Chairman of the Board, RISC-V International

As Chair, my role is to work with fellow Board members and our leadership team to set the organization's strategic direction, oversee our governance and structures, and ensure that RISC-V continues to grow as a single, open, and global standard that serves our members as well as the wider ecosystem.

On an annual basis, the Board agrees which specifications need to be prioritized or stabilized in the coming year, which areas of the ecosystem are most critical, and where we need to invest more effort. When profiles or major extensions come forward for approval, the Board looks at them from multiple angles:

Are they technically complete? Are they widely needed by the market? Do they help reduce fragmentation rather than increase it?

The aim is to give members and the broader ecosystem a clear, coherent package that they can implement with confidence.

This has been a year of steady, substantive progress, focused on sustaining the pace of innovation, improving accessibility for developers and maintaining an open standard.

Sustaining the Pace of Innovation

While RVA23 was ratified in 2024, I have been encouraged by the positive progress and adoption from companies embracing it as the single path forward throughout 2025. We have also advanced our technical roadmap, strengthened the ecosystem and taken important steps to position RISC-V for broader commercial deployment.

It is especially encouraging to see the volume of ratifications later in this report: they're tangible milestones towards productizing our ISA. In particular, the Server SoC spec gives us a much-needed baseline for server-class hardware, while RPMI and BRS standardize critical platform management and boot/runtime firmware services. And ratifying the Debug spec brings consistency to debugging, so tools work predictably and deliver fewer surprises for developers.

Much of what we have achieved this past year has been about laying stronger foundations, and I am optimistic about the opportunities ahead in 2026 as we build on this momentum and translate it into visible success across markets and regions.

Improving Accessibility and the Developer Experience

We want to make RISC-V International more accessible – for both our academic and commercial users. Many commercial users have less patience for "hackathon-like" workflows and expect familiar ways to find, read, and use technical documentation and information.

We want to improve the developer experience to be more professional, so it's easier for people to adopt and migrate to RISC-V. This is a key part of being more commercial-friendly and deployment-ready. We will also prioritize software ecosystem support, because success depends not only on the ISA specification but on the entire stack playing well together.

Maintaining a Single, Global, Open Standard

One of the clearest priorities the Board set for 2025 was to move the RISC-V ISA from being "de facto" recognized to being formally recognized in the international standards system. Becoming an ISO/IEC JTC 1 PAS Submitter, as Andrea noted in his foreword, is the gateway to that outcome.

From a Board perspective, this recognition has two important consequences. Firstly, it confirms that our governance, openness and processes already meet the expectations of the international standards community – and where gaps exist, we have used this process to strengthen RISC-V International as an organization. Secondly, it gives our members and their customers a clear pathway to seeing RISC-V treated in national and regional policy,

procurement and conformity-assessment frameworks on the same footing as other long-established technologies.

As we move into 2026, our focus will be on using this new status responsibly to ensure that international standardization becomes a genuine amplifier of global trust and interoperability.

Welcoming Our New CEO and VP of Technology

Following the departure of previous CEO Calista Redmond at the end of last year, the Board undertook a search for the next leader of RISC-V International in early 2025. We sought a leader with a technical interest and vision for RISC-V, strong execution skills, and the ability to set direction, gather input, refine plans, and deliver results. Just as important was the capacity to engage the community and the Board constructively, turning feedback into decisive action. Vitally, we were looking for passion. This was not just another corporate role; it was an opportunity to help reshape the computing landscape.

Andrea Gallo, who was promoted from VP of Technology to CEO in May 2025, embodies those qualities. In his first six months, he has engaged deeply with members across regions and market segments, listening carefully while also setting out a clear direction for RISC-V. The Board has confidence in his judgment and is encouraged by the energy and clarity he has brought to the role.

Of course, it was then necessary to backfill the VP of Technology role, to which we appointed industry veteran Tom Gall (ex-IBM, ex-Linaro) in November. The Technical Steering Committee led much of this process, as the VP of Technology works closely with technical leaders across the organization.

We were looking for someone who can understand complex technical discussions, mediate objectively between different viewpoints and help groups converge on practical solutions. Tom brings that balance of depth and neutrality, along with a strong track record of building and recruiting technical teams, and he has already started to provide a unifying technical perspective across our many workstreams.

Streamlining our Working Groups

RISC-V International has multiple types of committees and working groups, each with a different role – from technical advancement to regional governance. The Board sets overall strategy and approves major policy decisions, such as profiles, key technical baselines and important changes to the IPR policy. Technical committees and task groups then do the detailed work of designing and reviewing specifications, while a separate governance committee looks at organization-wide processes.

2026 Board Strategic Priorities at a Glance

RISC-V as a First-Class Citizen

The Board recognizes the need to ensure RISC-V competes technically with established commercial architectures, especially in demanding workloads.

We're advancing AI/ML and server capabilities by completing key extensions, clarifying accelerator interfaces and formal descriptions, and ratifying new specifications so implementers can build confidently on a robust, modern baseline.

Ecosystem Software Compatibility

A compatible software ecosystem lowers barriers to entry and allows innovation to scale across many different implementations of RISC-V. Alongside RISE we're building a unified ecosystem with stronger interoperability and shared enablement, so operating systems, toolchains and frameworks work seamlessly together across compliant RISC-V platforms.

Developer Experience via riscv.org

We're growing riscv.org as the primary hub for documentation, tools and guidance, simplifying navigation, consolidating resources, and providing structured onboarding paths and reference platforms that encourage developers to adopt RISC-V and move quickly from evaluation to deployment.

Commercialization & Advocacy

Success stories and clear market messaging help organizations confidently choose RISC-V for their next generation of products. We're aligning technical, marketing and policy efforts to support deployments in key verticals such as AI and automotive, showcasing proven solutions, and using targeted outreach and advocacy to highlight the benefits of RISC-V to industry and public-sector decision-makers.

Global Representation & Standards

Recognition in regional initiatives and international standards positions RISC-V as a trusted, long-term foundation for global innovation. We're strengthening engagement in priority regions, participating in relevant industrial and policy forums, and completing ISO and related standardization processes so organizations can adopt RISC-V with confidence.

Revenue & Budget Discipline

Our resilient, well-funded non-profit organization ensures that the RISC-V ecosystem is supported and stewarded for the long term. We're maintaining strict financial discipline so that RISC-V International remains a self-sustaining, globally trusted steward of the architecture.

Technical Updates

As a globally diverse, member-driven nonprofit organization with contributors spanning companies, regions, and time zones, RISC-V International does not operate like a traditional corporation with a top-down hierarchy or closed-door decision-making.

To make progress (and to measure it consistently) we rely on a clear, transparent technical structure. To achieve this, we have organized contributors into committees and groups, each with distinctly defined roles and responsibilities, so that hundreds of contributors can collaborate effectively and openly without conflicting paths or doubling up of workloads.

At the top of this structure sits the Technical Steering Committee (TSC), which sets overall technical direction, approves new work, and ratifies specifications. Beneath it, ISA Committees focus on instruction-set extensions, while Horizontal Committees (HCs) coordinate cross-cutting areas such as security, platform requirements, or software enablement.

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New Special Interest Groups (SIGs) and Task Groups (TGs) created in 2025

Most specifications are developed in Task Groups (TGs), which are formed to deliver a specific technical outcome. Special Interest Groups (SIGs) provide lighter-weight forums for discussion and alignment, without producing formal specs. Together, this taxonomy ensures community ideas are translated into stable, globally adopted standards.

2025 saw steady progress across multiple areas of the architecture. A number of specifications reached full ratification, covering platform management, firmware and boot flows, memory-management behavior, vector intrinsics, debugging, and server-class system definitions.

Ratification matters because it turns ideas and draft proposals into stable, agreed-upon standards that implementers can rely on with confidence; ensuring compatibility, reducing risk, and allowing software and hardware from different vendors to function predictably.

The following list captures all specifications formally approved in 2025.

Month Ratified	Extension Name	Description
January	Load/Store Pair for RV32	Improves how RISC-V handles memory operations by allowing two data words to be loaded or stored at once, effectively doubling throughput per instruction. The result is improved code density and reduced memory traffic, directly benefiting power- and cost-sensitive designs. It helps AI and signal-processing workloads too, where memory bandwidth is often the bottleneck rather than compute, especially at the edge.
February	Semihosting Specification	Enables early software to perform input/output and debugging through a host computer before the target device's own OS or drivers are ready. It significantly speeds up the bring-up process of new RISC-V-based products by allowing developers to test and refine code in simulation or prototypes, accelerating time-to-market for everything from IoT gadgets to complex aerospace systems.
	Server SoC Specification 1.0	Defines the baseline hardware, management, and security capabilities that any RISC-V server-class SoC must provide timers, interrupts, IOMMU, RAS, performance monitoring, and BMC connectivity aligned with standards like PCIe, ACPI, UEFI, and Redfish. This gives hyperscalers and OEMs a predictable, interoperable platform for data-center and AI workloads, reducing integration risk and TCO.
	Debug Specification 1.0	Standardizes how external debuggers connect to and control RISC-V chips, covering breakpoints, single-step, triggers, and system-level access. Defining a consistent debug interface across all RISC-V chips makes development and troubleshooting more straightforward. This gives tool vendors and silicon providers a single, stable target, reducing bring-up friction and improving reliability across markets from safety-critical automotive systems to cloud and AI infrastructure.

Month Ratified	Extension Name	Description
March	IO Mapping Table (RIMT)	Standardizes how a RISC-V system describes its hardware resources (like I/O and memory mappings) to an operating system. In practice, it allows mainstream OS software to detect and configure RISC-V hardware in the same straightforward way as on traditional server platforms (via industry-standard ACPI tables), smoothing RISC-V's path into data centers and other complex computing environments.
April	RVV C Intrinsics	Adds a high-level programming interface for RISC-V's vector processing, letting developers use data-parallel computations without writing low-level assembly. By simplifying vector acceleration, it boosts performance for demanding applications in artificial intelligence and multimedia. Industries from edge AI devices to high-performance computing benefit, as software can readily leverage RISC-V's vector capabilities.
June	Address Range Invalidation	Gives software fine-grained control to invalidate specific ranges in I/O memory mappings (IOMMUs) rather than clearing everything. Such targeted memory management improves system-level efficiency, which is critical for high-throughput environments. It means RISC-V servers and virtualized systems can handle data movement and device virtualization with less overhead, directly benefiting cloud providers and any data-intensive operation.
	Non-leaf PTE Invalidation	Ensures correctness in complex memory virtualization by clarifying how to invalidate higher-level entries in multi-level page tables. In simpler terms, it fortifies RISC-V's ability to run virtual machines and secure OS partitions reliably. This is key for cloud computing and any industry (like automotive) that relies on robust isolation between software components for safety and security.

Month Ratified	Extension Name	Description
July	Supervisor Binary Interface 3.0	Modernizes the interface between RISC-V platform firmware and operating systems (and hypervisors). A cleaner, well-defined SBI means OS software can fully leverage RISC-V features and virtualization with fewer custom fixes. For enterprise and cloud uses, it ensures smoother RISC-V support in servers and simplifies building complex multi-OS platforms across industries.
	Platform Management Interface: RPMI (1.0)	Establishes a unified way for RISC-V systems to report and control platform health metrics,covering power levels, temperatures, and system status. A common management interface means operators can manage RISC-V–based servers at scale just as easily as existing architectures. It also aids industries like automotive, which demand consistent monitoring of system health for safety and performance.
August	Boot & Runtime Services (BRS)	Standardizes the firmware services needed to boot and run RISC-V systems, much like how PCs have a uniform BIOS/UEFI. This consistency eliminates custom boot-code quirks, so operating systems can start on any RISC-V hardware with minimal adjustment. It speeds up RISC-V adoption across domains (from data center servers to consumer electronics), by ensuring predictable, reliable startup behavior.
	PTE Reserved-for-Software Bits 60–59	Reserves two bits in RISC-V page tables exclusively for software, ensuring they remain available across future processors. In practice, it lets operating systems employ those bits for advanced memory management or security features without fear of hardware conflict. This change future-proofs RISC-V for new virtualization and protection capabilities needed in both data center and embedded markets.
October	Load-Acquire/ Store-Release	Introduces simple but powerful memory synchronization instructions (Load-Acquire and Store-Release) into RISC-V, ensuring multi-threaded software runs in the correct order without heavy performance penalties. In practice, it makes multi-core RISC-V systems easier to program correctly and efficiently. From cloud databases to edge AI devices, developers get a straightforward way to achieve reliable parallel performance with less complexity.

Community Programs

From high-school students and hobbyists to multi-national corporations, our member community is the engine that drives RISC-V's progress.

Today, paid members range from academia to pre-seed startups to multinational corporations – the team works tirelessly to encourage companies that compete in the market yet share similar goals to share knowledge, build tools, improve specifications, and support newcomers.

But it's in our outreach to those still in education, academia or simply sitting coding in their bedrooms that much of the magic really happens. From students and researchers to hobbyists and educators, we believe the key is to meet them where they are. Through learning resources, local events, and chances to collaborate on real projects, RISC-V International helps anyone, anywhere to discover RISC-V, benefit from open technology, and play their part in shaping the future of this ecosystem.

The RISC-V community demonstrated remarkable momentum, leadership, and global collaboration in 2025. Ambassadors and Advocates were especially active, collectively hosting more than 100 events; expanding awareness and deepening engagement across the ecosystem.

These included multi-city activities like World RISC-V Days across Beijing, Hong Kong, Japan, Taipei and Vietnam, as well as in-person and online hackathons, regional meetups, and our 'Open Hours' virtual events that highlighted ongoing technical progress.

Our mentorship programs played a pivotal role in workforce development, providing hands-on experience for 49 participants. Several mentorships translated directly into full-time roles within member organizations; clear evidence of the program's impact and the growing demand for skilled RISC-V talent.

2025 also marked a major milestone with the launch of our first developer workshops. Sessions were hands-on, lasting one to two hours, and were extremely well received, giving practitioners opportunities to dive deeper into key technical topics and strengthen connections across the community.

Additionally, we expanded our Featured Work initiative, reviewing poster sessions in person at RISC-V Summits and selecting standout projects for short video features and accompanying write-ups published on the RISC-V blog. This effort has helped spotlight some of the most innovative work in the ecosystem and elevate emerging contributors, and we'll be continuing this drive with renewed vigor in the new year.

Overall, 2025 showcased a community that is not only growing, but actively shaping the future of open computing through education, collaboration, and shared innovation.

Global Events

Organizing the RISC-V Summits and participating in key industry and community events as an exhibitor are essential to accelerating ecosystem growth. These forums allow us to meet engineers where they are, demonstrate real silicon and software progress, and connect members with prospective adopters.

In 2025, our physical presence at global events was more critical than ever. These events let us tell a consistent story: RISC-V is an open standard, globally supported, and ready for serious products. It also enables us to hear first hand what developers, integrators, and decision-makers in specific key markets need next.

From dedicated regional summits to well-established open-source and vertical market trade shows and region-specific ecosystem gatherings, we invest in booths, demos, technical sessions, and networking to raise awareness, highlight member innovation, and showcase real-world implementations of RISC-V technology.

Embedded World 2025

Nuremberg, Germany

March 11–13, 2025

As the world's largest trade fair for embedded technologies, Embedded World 2025 drew approximately 32,000 visitors and 1,200 exhibitors to Nuremberg, serving as the primary meeting place for the global embedded community. The event focuses on security, electronic displays, and distributed intelligence (edge AI), attracting a highly technical audience of system designers and engineers. RISC-V International anchored a dedicated pavilion presence: a 10m × 10m open-sided booth in Hall 5 featuring a presentation theater, developer zone, meeting areas, and six demo pods.

Our impressive pavilion hosted six member companies: Andes, DeepComputing, Semidynamics, Siemens, SiFive, and Synopsys. Each demonstrated cutting-edge RISC-V IP, AI solutions, development tools and consumer products.

Beyond the exhibition floor, we hosted two well-attended "powered by RISC-V" conference sessions on development and system design, alongside a packed schedule of theater talks at our booth. To broaden visibility, we distributed "WE ARE A RISC-V MEMBER" signage to fellow exhibitors, culminating in a networking soiree offering beer and wine at our booth.

RISC-V Summit Europe 2025

Paris, France

May 14–16, 2025

RISC-V Summit Europe has established itself as the premier RISC-V-focused convening point in Europe, held at the Cité des Sciences et de l'Industrie.

The summit emphasized Europe's accelerating adoption of RISC-V across markets such as automotive, embedded, and AI, while also providing structured "on-ramps" (Intro to RISC-V) for newcomers. Over the three days, the event attracted 710 registered attendees from across Europe. The robust program featured 12 keynotes, 44 plenary sessions and 29 demos and multiple tutorials, and working group sessions, offering deep technical insight.

Of particular note was our poster program, with more than 180 posters displayed across three days by academia and startups. In addition to core conference programming, RISC-V International facilitated networking opportunities (including the new "RISC-V Hot Topics Table Talk" and a community breakfast panel featuring insights from RISC-V ambassadors).

The event culminated in a memorable reception and buffet dinner at the science museum, granting attendees private access to its exhibits.

Computex 2025

Taipei, Taiwan

May 20-23, 2025

The RISC-V Pavilion on the Computex show floor brought together 12 exhibitors, including Andes Technology, Tenstorrent, Skymizer, Syntronix, RISE Project, DeepComputing, Nuclei System Technology, Semidynamics, Alibaba DAMO Academy and others.

We were pleased to see such a strong, coordinated demonstration of real-world silicon, software, and system-level innovation.

Across the pavilion, AI and edge computing were front and center, with multiple examples of RISC-V designs tightly integrated with NPUs and other accelerators. RISC-V Taipei Day, held for the first time at Computex, reinforced this momentum.

DeepComputing's unveiling of the DC-ROMA RISC-V AI PC, delivering over 40 TOPS of local AI performance on Ubuntu Desktop 24.04 LTS, was a standout moment that resonated strongly with attendees.

Technical sessions on RVV 1.0, functional safety, and security highlighted how an open ISA enables both performance and trust. Collectively, the week reinforced to us, and to the wider audience, how essential openness and collaboration are to scaling AI computing beyond the cloud.

Open Source Summit USA 2025

Denver, Colorado, USA

June 23–24, 2025

The Linux Foundation's Open Source Summit is the leading conference for open-source developers and community leaders in North America, making it a critical venue to align hardware standards with software ecosystems and reinforce RISC-V's messaging around upstream collaboration and open innovation.

As a Bronze sponsor, RISC-V International focused on bridging the gap between hardware innovation and open software communities.

The team hosted a mini-summit, titled 'RISC-V & Yocto: Your On-Ramp to Open Innovation', featuring four community speakers who highlighted the synergy between the two projects.

Our booth traffic was boosted by a popular Banana Pi raffle, while technical engagement was bolstered by well-attended sessions and Learning Lounge talks.

Notably, we leveraged the Unconference format to host an open discussion on RISC-V, which recorded the highest attendance of any unconference track, signaling a massive appetite for direct dialog about the architecture.

RISC-V Brazil Event 2025

Campinas, Brazil

July 3–4, 2025

RISC-V Brazil is a fast-growing regional convening point bringing together academia, research institutes, industry, and government to strengthen cooperation around the RISC-V ecosystem in Brazil and across Latin America. Hosted at the Eldorado Research Institute in Campinas, the event's second edition saw expanded international engagement, with participants and speakers from Europe, the United States and China alongside a strong Brazilian contingent from universities, research centers, and industry.

The program opened with Eldorado and Brazil's Ministry of Science, Technology and Innovation, then moved into ecosystem and industry sessions spanning silicon, software, and real-world deployments. Presentations featured companies including Ventana, Red Hat, and Qualcomm, with strategic national organizations such as Embraer and Petrobras exploring adoption pathways in HPC, aerospace, and energy. Academic contributions highlighted initiatives like blueMACAW and RISC-V programs at USP, UnB, and Unicamp. Led by Diamond sponsor Ventana Microsystems and with institutional support from the Ministry, the event underscored RISC-V's growing role in regional innovation and technological sovereignty.

RISC-V Summit China 2025

Shanghai, China

July 17–19, 2025

One of the largest events in our global calendar, RISC-V Summit China welcomed a record-breaking 3000+ attendees from 17 countries at the Zhangjiang Science Hall, underscoring both China's domestic momentum and its importance to the global ecosystem. The summit featured a main forum plus multiple vertical technical forums focused on high-demand sectors including AI, High Performance Computing (HPC), and Automotive Electronics.

The headline news of the event was NVIDIA's CUDA announcement, validating the architecture's readiness for HPC. The event also included a large "Future Tech Exhibition Zone" reflecting the breadth of silicon, tooling, and platform activity in the region. The event also featured a number of launches of high-performance domestic cores and cutting-edge demos. The scale of the event, combined with heavy industry support, underscored China's role as a major driver of RISC-V volume and innovation, with sessions covering everything from embedded systems to next-generation data center technology.

RISC-V International's role centered on supporting our key vertical markets, amplifying member announcements, and alignment on software and standards.

World RISC-V Days 2025

Worldwide

August 4–8, 2025

World RISC-V Days is a synchronized, community-led week designed to bring the global RISC-V ecosystem together through locally hosted meetups running in the same time window worldwide. Its mission is explicitly about accelerating ecosystem growth and adoption across all regions, with special emphasis on emerging and smaller-scale communities that benefit most from shared visibility and practical support.

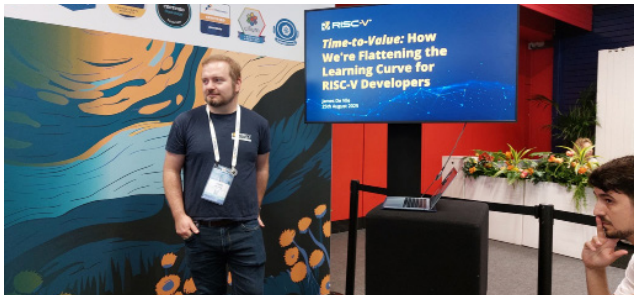
In its inaugural year, events spanned geographies including Hong Kong, Hsinchu City (Taiwan), Hanoi (Vietnam), Karachi and Lahore (Pakistan), India (Bangalore), Tokyo (Japan) and Beijing (China). Each event was tailored to local audiences and varied by audience size, yet united the community under one RISC-V Days banner.

RISC-V International's role was to coordinate, amplify, and connect these nodes – promoting the week, highlighting partner participation, and capturing outcomes. Following the strong response, RISC-V International created a dedicated hub page to showcase 2025 activity and maintain momentum towards next year's events.

Open Source Summit Europe 2025

Amsterdam, Netherlands

August 25–27, 2025



Open Source Summit Europe serves as the gathering place for the European open-source community, bringing together open source developers, technologists, and community leaders to explore a wide range of topics from Linux kernel development to AI ethics. RISC-V International prioritized interactive collaboration at this event to deepen ties with software developers.

We partnered with DeepComputing, Zephyr, and Framework to create a "passport" challenge, where attendees visited all four booths to win daily prizes. This gamified approach kept the RISC-V booth incredibly busy and facilitated meaningful conversations about hardware-software integration.

The booth program was complemented by educational content; we hosted a well-attended Learning Lounge talk, offering an accessible entry point for software engineers looking to understand the RISC-V ISA.

The event reinforced our close alignment with the open-source software community, encouraging its use of RISC-V as the default hardware choice for open software projects.

RISC-V Automotive Conference 2025

Munich, Germany

September 9, 2025

The first RISC-V Automotive Conference, held adjacent to the IAA Mobility show in Munich, Germany in September and jointly hosted by RISC-V international and Infineon. Following the theme "Shaping the Future of Mobility with Open Standards and Strong Partnerships", the event was attended by a number of OEMs, Tier-1 suppliers, and technology providers, and supported by ecosystem partners including Synopsys, MIPS, Hightec, Lauterbach, Green Hills Software, Tasking, PLS, Qt, MathWorks, and Quintauris.

The program explored how RISC-V can support software-defined vehicle (SDV) architectures by enabling differentiated compute across zonal controllers, ADAS, and in-vehicle edge AI. Executive keynotes and technical panels were complemented by an expo area that showcased practical ecosystem progress.

Networking was central throughout, with structured breaks designed to connect engineers and decision-makers and move conversations from interest to action. By anchoring a RISC-V-focused forum inside IAA week, RISC-V International helped align stakeholders around shared priorities, credible roadmaps, and concrete next steps for collaboration.

RISC-V Summit North America 2025

Santa Clara, California, USA

October 21–23, 2025

The flagship RISC-V Summit North America returned to Silicon Valley, drawing 975 attendees, with more than 25% in executive leadership roles and strong participation from Europe, Asia, America, and Australia.

The three-day conference opened with Member Day programs including RISC-V 101, workshops, technical sessions and (new for 2025) a Developer Workshop. The summit featured a packed agenda of 15 keynotes, 48 sessions, and 25 posters. RISC-V luminaries Krste Asanović and David Patterson joined leaders from Google, AWS, and the Linux Foundation, reflecting the ecosystem's growing mainstream momentum.

A key moment was CEO Andrea Gallo's update on the first steps RISC-V is taking toward international standardization. On the show floor, the sponsor expo and Developer Zone enabled live demos, technical deep dives, and high-value partner discussions, showcasing real-world products and ready-to-deploy solutions.

As the year's highest-density gathering of RISC-V stakeholders, the summit served as a critical alignment point – validating direction, surfacing integration challenges, and spotlighting launches across embedded through infrastructure-class compute.

RISC-V Ambassadors

Florian 'Flo' Wohlrab, CEO OpenHW Group and RISC-V Ambassador

Beyond our headline exhibitor presence, the RISC-V International team attended key regional and technical conferences and forums throughout 2025, including the IEEE Latin America & the Caribbean Semiconductor Summit (LACSS) and the GROW conference in Brazil, and the Semiconductor Workshop in Selangor, Malaysia. These targeted visits helped us better understand regional supply-chain dynamics, align with local priorities, and forge deeper connections with engineers, researchers, and decision-makers in these regions.

A small team, however, we can't be everywhere on the global tech calendar. That's why we rely on (and deeply appreciate) the wider community to extend RISC-V's presence and voice. In particular, our RISC-V Ambassadors attend events, convene local meetups, and host sessions that keep the ecosystem connected and visible worldwide.

Ambassadors are RISC-V experts from around the world who are leaders in their area of expertise. Successful Ambassadors include engineers and developers, who are actively contributing to work groups, community events, training, workshops, and more.

A recent example is SC25, the world's largest supercomputing conference, at which members of the RISC-V HPC Special Interest Group (SIG) represented the community (in lieu of RVI's attendence) and ran a panel session alongside broader RISC-V for HPC activity during the week.

Whether through a flagship pavilion or a handshake on the conference floor, RISC-V International and its ambassadors remain committed to meeting the community where it is, amplifying member innovation, and driving the open standard forward worldwide.

Thank You

RISC-V International is, at its core, a community-led organization. This past year's progress is a direct reflection of the people who show up, lean in, and do the work. We extend our sincere thanks to our Board, and to our Technical Steering Committee members for their steady leadership, thoughtful guidance, and commitment to keeping RISC-V's technical direction open, rigorous, and globally relevant.

We are equally grateful to our workgroup members, our chairs, and our ambassadors, whose energy and persistence turns plans into momentum. By convening contributors, aligning on priorities, and helping new participants find their footing, they play an outsized role in driving the growth of the ecosystem and strengthening collaboration across regions and industries.

To our paid members and event sponsors: thank you for your continued investment, advocacy, and support throughout the year. Your backing helps scale programs, sustain critical infrastructure, fund events that bring us face to face with the industry's brightest and best, and broaden participation across the community.

And last but by no means least, thank you to every individual engineer, researcher, educator, student, and volunteer who contributed their time, expertise, reviews, code, and ideas. RISC-V moves forward because of the collective effort, and we owe its ongoing success to each and every one of you. Because open standards are strongest when we come together.

Join RISC-V International

Help shape the future of computing together. As a member, you'll have the opportunity to collaborate with industry peers, influence an open global standard, accelerate development and maintain a competitive edge in the rapidly evolving tech landscape.

To learn more, visit https://riscv.org/members/join/

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